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MULTITHRESHOLD CMOS SLEEP STACK AND LOGIC STACK TECHNIQUE FOR DIGITAL CIRCUIT DESIGN

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ABSTRACT

Power optimization is the major problem in digital circuit design. In this paper using MTCMOS and stack techniques are proposed. Multi threshold CMOS sleep stack and logic stack, super cutoff sleep stack and logic stack are proposed. Stacking is introduced in MTCMOS concept which decreases leakage power based on the power dissipation of pMOS and nMO Stransistor. MTCMOS technique uses multiple voltages in the circuit which is the main advantage of this. Power dissipation, propagation delay and power delay product are calculated. Constrains like power, delay is compared with the existing techniques. It is proved that proposed technique is better than previous technique. Simulation results are given using HSpice.

Keywords: propagation delay, power dissipation, multi-threshold, leakage.

1. INTRODUCTION

Electronic device with battery backup is trending fastly. So it's a challenging task to design the digital circuits with low power dissipation and delay. If the concentration goes on power, speed decreases due to some constraint. So it is significant to meet both power and delay simultaneously. This MTCMOS concept pays for the issue. Multi threshold CMOS sleep and logic stack technique provides a considerably less power dissipation and delay. Super cutoff multi threshold technique provides better power performance than the previous.Components of static power dissipation are junction leakage, gate induced drain leakage, punch through leakage, sub-threshold leakage, gate-oxide leakage and hot carrier injection currents. Leakage current is mainly caused by subthreshold leakage current [3]. This occurs because of leakage in steady state that is before reaching the threshold voltage of the device. So multi threshold is the concept which reduces the leakage. That is giving different gate voltage to the transistors.

2. EXISTING STACK TECHNIQUE FOR LEAKAGE POWER REDUCTION

Manish Kumar, Md. Anwar Hussain, Sajal K. Paul (2013) describes these techniques

A. Hybrid multi-threshold CMOS complete stack technique

High threshold voltage is given to the pMOS and nMOS sleep transistor which are placed between vdd and logic circuit pull up network, pull down network of logic circuit and ground respectively in this technique as shown in Figure-1. Then all the transistors that is both logic circuit and sleep transistor are stacked in the circuit [1, 7].

B. Hybrid multi-threshold partial stack technique

High threshold voltage is given for sleep transistor and low threshold voltage for logic circuit same as complete stack method but stacking of transistor differs. Only sleep transistor are stacked not the logic circuit as shown in Figure-2. So this technique gives low power dissipation than the complete stack [1].

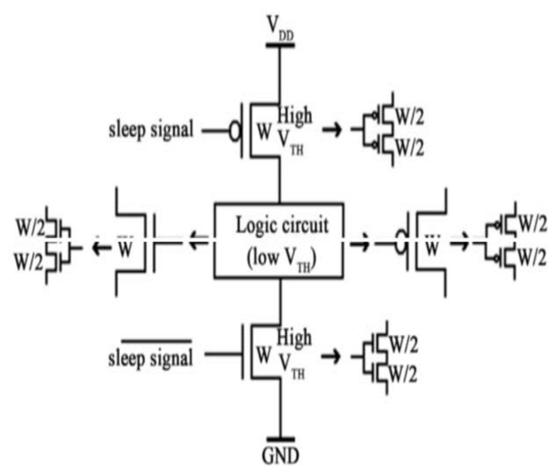

Figure-1. Hybrid MTCMOS complete stack technique.

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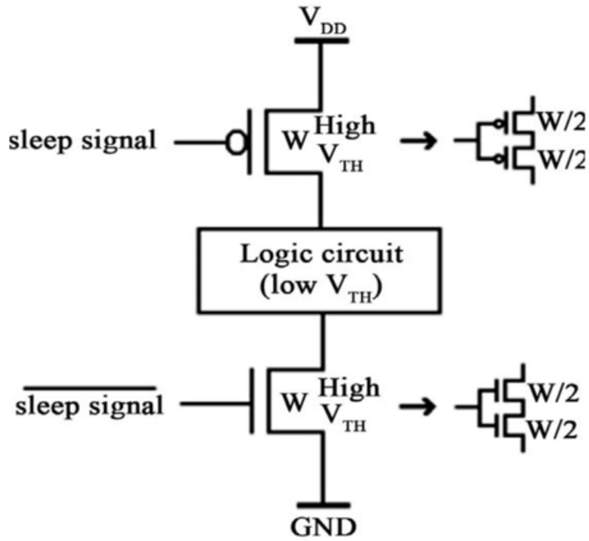

Figure-2. Hybrid MTCMOS partial stack technique.

C. Hybrid super cutoff complete stack technique

Hybrid super cutoff technique is similar to hybrid multi-threshold CMOS complete stack technique. The modification is no high threshold voltage is used; only low threshold is used which is shown in Figure-3. That is for both logic circuit and sleep transistor low threshold is used. In active mode the low *VTH* sleep transistors are in off state. Because of this there is low resistance input-output path [1]. This reduces the propagation delay of the circuit as compared with hybrid multi-threshold stack technique.

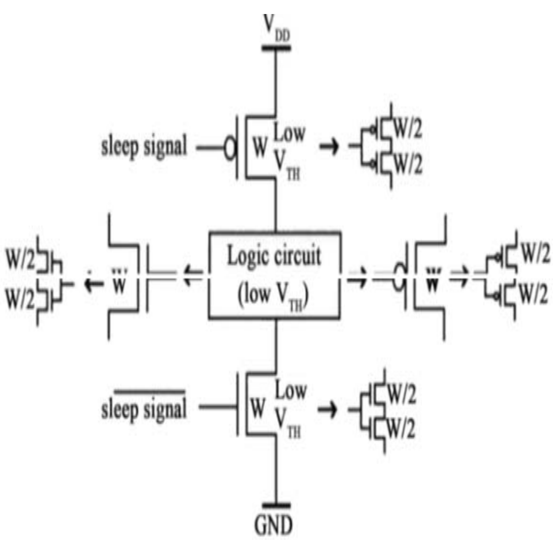

Figure-3. Hybrid super cutoff complete stack technique.

D. Hybrid super cutoff partial stack technique

Hybrid super cutoff partial stack technique is similar to hybrid multi-threshold CMOS partial stack technique. The only change is use of low threshold voltage instead of high threshold voltage for sleep transistors. Here stacking is done for sleep transistor alone not for the logic circuit also as show in Figure-4. So it is called as partial stack method. This super cutoff technique gives less power dissipation than the hybrid multi-threshold CMOSstack technique [1]. As only low threshold is used it is better than the previous hybrid multi-threshold CMOSstack technique.

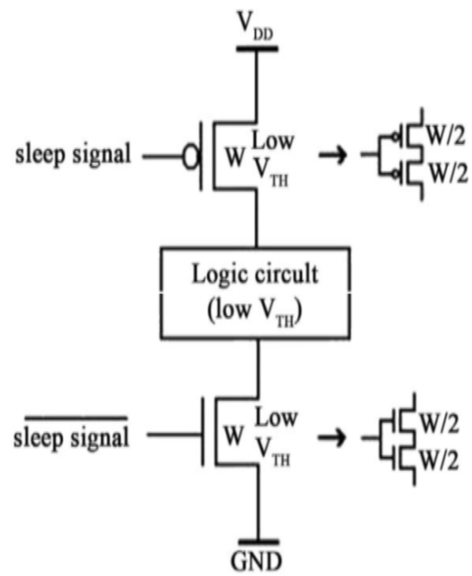

Figure-4. Hybrid super cutoff partial stack technique.

3. PROPOSED MTCMOS STACKING TECHNIQUE

A. MTCMOS sleep pMOS stack and logic nMOS stack technique

High threshold voltage is given for pMOS and nMOS sleep transistor. Low threshold voltage is given for logic circuit. Sleep transistor pMOS is stacked with two transistors instead of one transistor. The width is divided by two [7, 8]. Then the logic circuit nMOS is stacked similarly [2]. In Figure-5 sleep transistor nMOS and logic circuit pMOS are not stacked. In sleep mode the pMOS sleep transistor will turned on which is stacked and the logic circuit stacked nMOS will turn off. This increases the resistance of leakage path which reduce the power dissipation of the circuit [2, 10].

B. MTCMOS sleep nMOS stack and logic pMOS stack technique

High threshold is used for sleep transistor and low threshold is for logic circuit. NMOS sleep transistor is stacked with two transistors and pMOS logic circuit is stacked as shown in Figure-6. In sleep mode the stacked

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sleep nMOS transistor will turn off. This reduces the leakage power dissipation of the circuit [10].

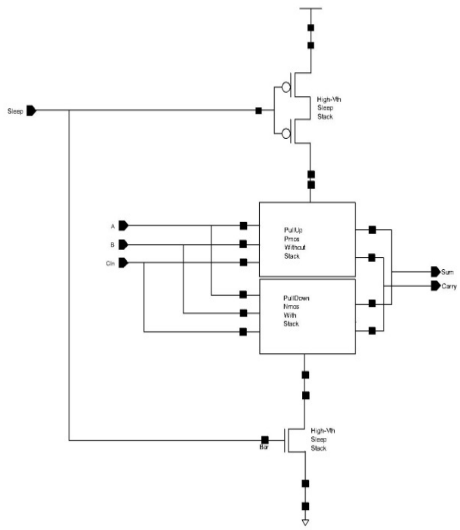

Figure-5. Full adder circuit using MTCMO sleep pMOS stack and logic nMOS stack technique.

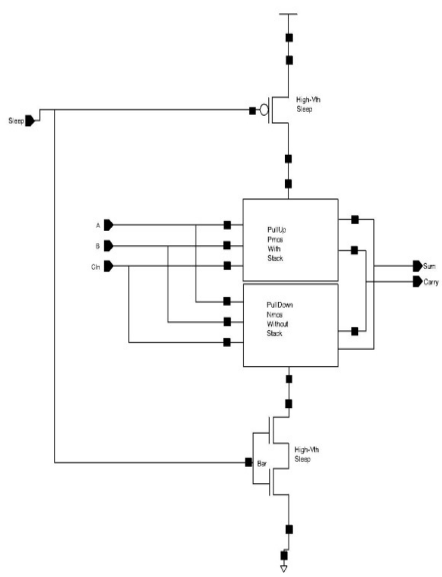

Figure-6. Full adder using MTCMOS sleep stack and logic pMOS stack technique.

C. MTCMOS sleep pMOS stack and logic pMOS stack technique

pMOS and nMOS sleep transistor are given high threshold voltage which is placed between pull up network and vdd, logic circuit pull down network and ground. Low threshold voltage is used for circuit as shown in Figure-7. Sleep transistor above logic circuit is stacked and logic circuit pull up network is stacked.

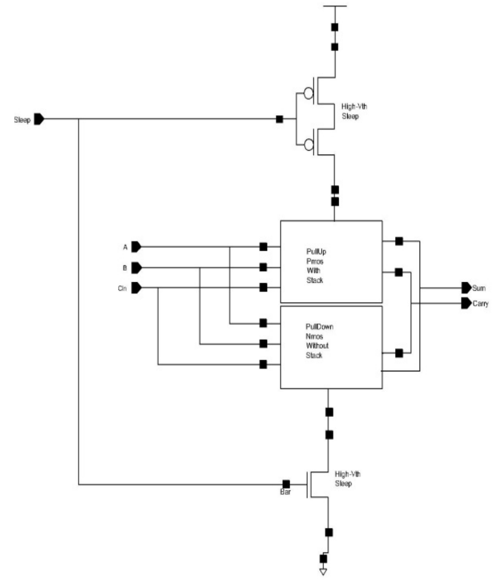

Figure-7. Full adder using MTCMOS sleep pMOS stack and logic pMOS stack technique.

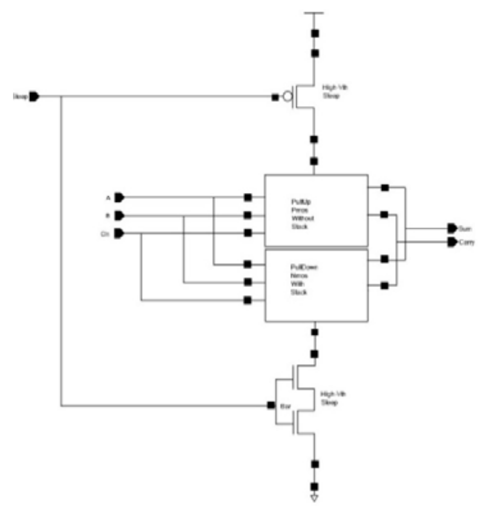

Figure-8. Full adder using MTCMOS sleep nMOSstack and logic nMOS stacking technique.

D. MTCMOS sleep nMOS stack and logic nMOS stack technique

Threshold voltage given to the circuit is same as the previous technique. In this nMOS sleep transistor which is placed between output and ground is stacked. Logic circuitpull down network is stacked [6, 9]. In sleep mode the nMOS sleep transistor is in off state. So there is no direct leakage in the circuit. Circuit is shown in Figure-8.

4. PROPOSED SUPER CUTOFF STACKING TECHNIQUE

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A. Super cutoff sleep pMOS stack and logic nMOS stack technique

Technique is similar to MTCMOS sleep pMOS stack and logic nMOS stack technique. In this technique pMOS sleep transistor is stacked. In this low threshold voltage is used. High threshold is not used as shown in Figure-9. So it works in super cutoff region. In sleep mode the pMOS sleep transistor is turned on and the nMOS sleep transistor is turned off. Use of both negative and positive voltage reduces the power dissipation exponentially [5, 9].

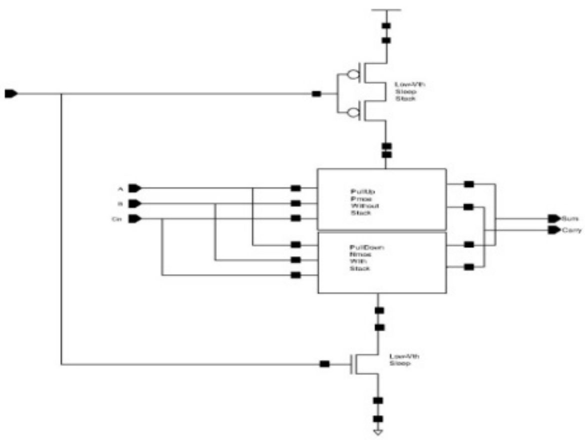

Figure-9. Full adder using super cutoff sleep pMOS stack and logic nMOS stacking technique.

B. super cutoff sleep nMOS stack and logic pMOS stack technique

Only low threshold voltage is used in this technique. The nMOS sleep transistor is stacked. In sleep mode nMOS sleep transistor is switched off. That is the stacking of nMOS is done by replacing the transistor by two transistors with width of w/2 [7]. In this logic pMOS is also stacked which reduces the leakage power by increasing the resistance of guiding path. This is similar to MTCMOS sleep nMOS stack and logic pMOS stack technique as this is shown in Figure-10.

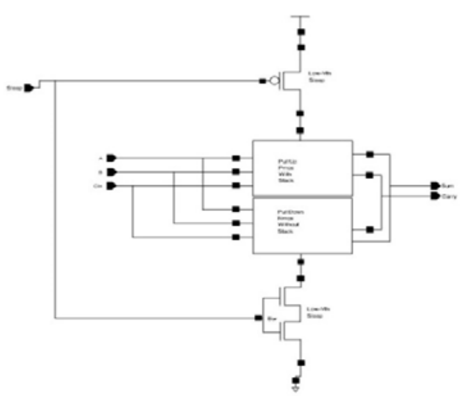

Figure-10. Full adder using super cutoff sleep nMOS stack and logic pMOS stacking technique.

C. Super cutoff sleep pMOS stack and logic pMOS stack technique

Super cutoff sleep pMOS stack and logic pMOS stack technique is similar to mtcmos sleep pMOS stack and logic pMOS stack technique. The only difference is use of low threshold voltage for both sleep transistor and logic circuit propagation delay is reduced by the use of two voltages to pmos and nmos sleep transistor as shown in Figure-11.

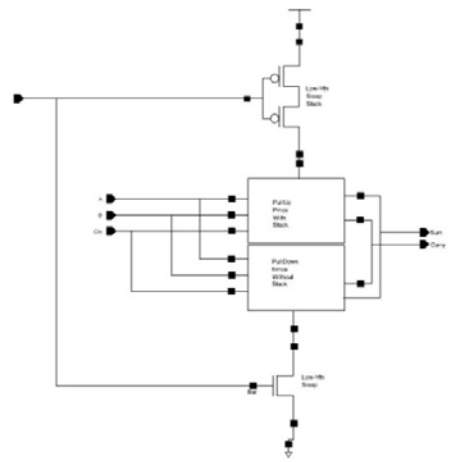

Figure-11. Full adder using super cutoff sleep pMOS stack and logic pMOS stacking technique.

D. Super cutoff sleep nMOS stack and logic nMOS stack technique

NMOS sleep transistor is stacked with two transistors. This stacking of transistor in series makes the circuit more resistance to leakage power [4]. The only use of low threshold increases the speed of the circuit by reducing the propagation delay. It is similar to MTCMOS sleep nMOS stack and logic nMOS stack technique as shown in Figure-12.

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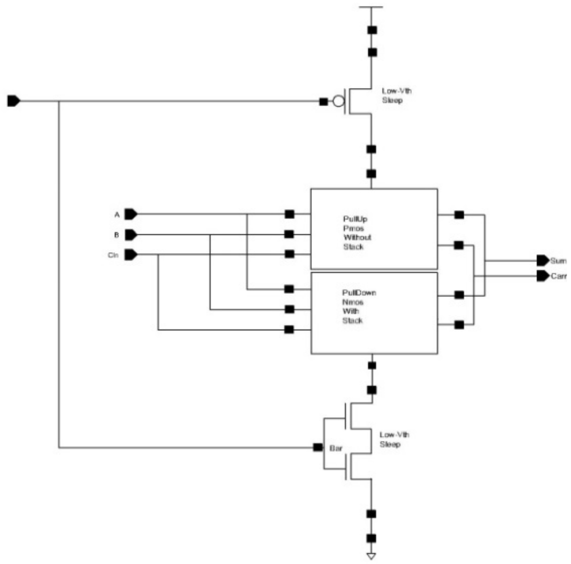

Figure-12. Full adder using super cutoff sleep nMOS stack and logic nMOS stack technique.

5. RESULT AND DISCUSSIONS

Full adder circuit is used to analyze the proposed techniques. The outputs of the proposed techniques are given using HSpice. The output is plotted across time and voltage. The power analysis of the circuits is done. The parameters like power, delay, and power delay product are measured.

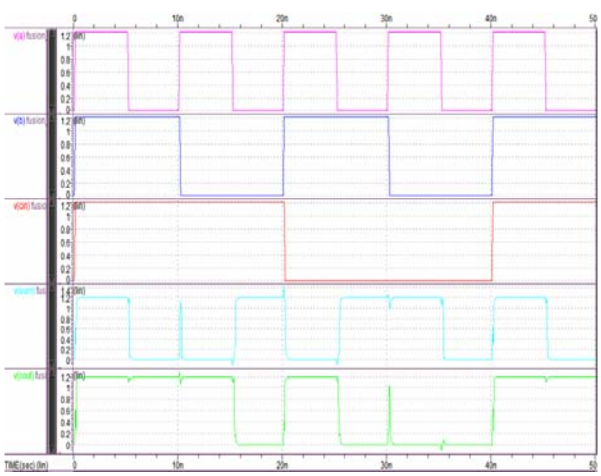

Figure-13. Full adder output waveform using MTCMOS sleep nMOS and logic pMOS stacking technique.

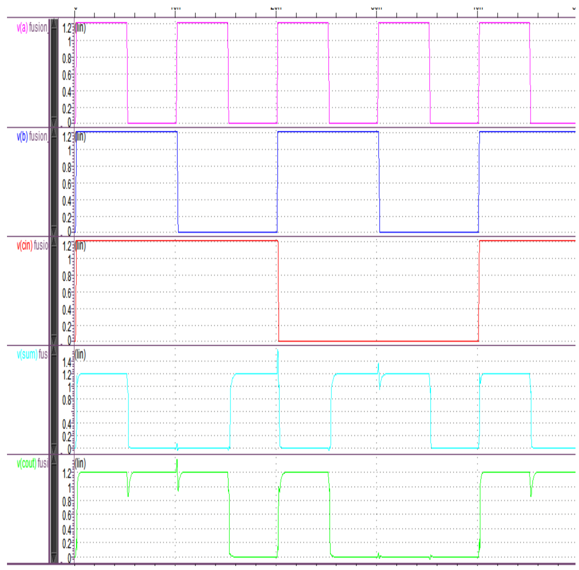

Figure-14. Full adder output waveform using MTCMOS sleep pMOS and logic nMOS stacking technique.

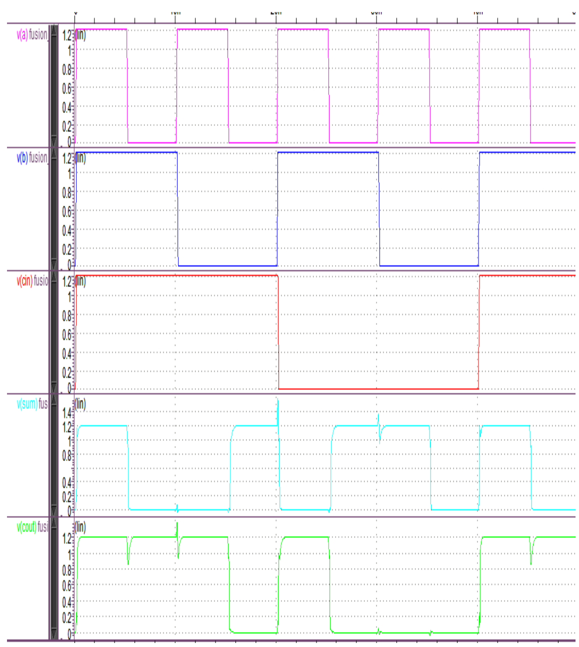

Figure-15. Full adder output waveform using super cutoff sleep nMOS and logic pMOS stacking technique.

Figure-16. Full adder output waveform using super cutoff sleep nMOS and logic pMOS stacking technique.

Table-1. Performance analysis of existing and proposed leakage power reduction techniques.

	Methods	Average power	Average delay	Power delay product
Existing methods	Hybrid MTCMOS complete stack technique	4.2820µW	5.1374ns	16.8607fJ
	Hybrid MTCMOS complete stack technique	4.7117µW	5.2343ns	24.1168fJ
	Hybrid super cutoff complete stack technique	3.2746µW	5.2349ns	16.8300fJ
	Hybrid super cutoff complete stack technique	1.0228µW	5.9332ns	15.2321fJ
Proposed method	MTCMOS sleep pMOS and logic nMOS stacking technique	3.9276µW	5.1099ns	20.0699fJ
	MTCMOS sleep nMOS and logic pMOS stacking technique	3.6069µW	5.1192ns	23.5839fJ
	MTCMOS sleep pMOS and logic pMOS stacking technique	4.0308µW	5.1683ns	26.0008fJ
	MTCMOS sleep nMOS and logic nMOS stacking technique	3.6570µW	4.0827ns	18.5875fJ
	Super cutoff sleep pMOS and logic nMOS technique	0.5036µW	5.0914ns	2.5640fJ
	Super cutoff sleep nMOS and logic pMOS technique	0.6511µW	5.1501ns	5.7338fJ
	Super cutoff sleep pMOS and logic pMOS technique	0.8994µW	5.1503ns	4.6325fJ
	Super cutoff sleep nMOS and logic nMOS technique	0.9721µW	5.0881ns	4.9468fJ

6. CONCLUSIONS

Leakage power is a major problem nowadays that to subthreshold leakage is the predominant factor that challenges the circuit designers. MTCMOS sleep stack and logic stack technique provides a solution for this problem. When comparing with this technique super cutoff sleep stack and logic stack technique is superior. Full adder circuit is used to compare the performance of these techniques. Leakage power is reduced to greater extent than the existing method. Comparing with existing hybrid MTCMOS partial stack technique the proposed MTCMOS sleep nMOS and logic pMOS stacking technique achieved 13.88% of improvement in power reduction, 16.63% of improvement in delay reduction, and 22.92% of improvement in power delay product. The proposed super cutoff sleep pMOS and logic nMOS technique achieved 84.62% improvement in power reduction, 1.55% of improvement in delay reduction, and 84.76% of improvement in power delay product.

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