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HIGHLY RELIABLE LOW POWER MAC UNIT USING VEDIC MULTIPLIER

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ABSTRACT

An efficient high performance 64-bit MAC unit (Multiplier-and-Accumulator) is presented. In most of the applications Multiplier and Accumulator plays an important role. The existing method is designed using Braun, dadda, etc., like different multiplier architecture and compared the performance of MAC unit with those multipliers. Hence it is vital to design a high-performance multiplier to meet the needs like high speed, less delay, low cost and reduced power. Therefore the proposed method is 64-bit MAC unit which is designed using Vedic multiplier using URDHVA-TIRYAKBHYAM sutra. The main objective of this work was to get an efficient MAC unit with less delay and reduced power. Hence the MAC unit is analyzed using XILINX ISE 13.2 in Verilog HDL and simulated using MODELSIM SE 6.3g and QUARTUS II 9.0.

Keywords: MAC unit, vedic multiplier, URDHVA_TIRYAKBHYAM, less delay.

INTRODUCTION

The MAC unit is nothing but a combination of Multiplier and Accumulator which contains the sum of the previous successive products. The MAC inputs are given to the multiplier block after obtaining the inputs from the memory location. It provides high speed multiplication saturation and clear-to-zero function. MAC unit operation is the key operation of most of the high performance systems like microprocessors, FIR filters, etc. [6] this paper work is organized into nine sections as follows.

In the first section it briefs about introduction and in section 2 and 3, it discuss about the operation of Multiplier-Accumulator and performance of Vedic multiplier based on Urdhva-tiryakbhyam sutra. In section 4, it describes the implementation of MAC unit based different multiplier architectures and their comparison in-terms of better performance [9]. In section 5, it details about the performance of proposed MAC unit based on the modified adder circuit and in section 6, 7and 8 the obtained results are analyzed respectively and finally conclusion is made in the ninth section.

A system's performance is mainly determined by means of the multiplier performance in general because, the multiplier is the slowest element in a system and in general it is most area consuming in a system.

Hence as a result an efficient MAC unit is designed using the Vedic multiplier by modifying the adder circuit in the MAC unit [7]. Therefore Multiplier-Accumulator construction plays an important role in our work because we have choosen the Vedic multiplier which produces better performance than the one which is implemented previously in the MAC unit architecture.

MAC OPERATION

Hence the MAC unit operation is the key function in multimedia information processing and also in different other applications. Generally the architecture of MAC unit consists of adder, multiplier and accumulator. [1] The delay can be reduced by building the adder and accumulator in the same block in this paper for better performance. Hence it is useful in signal processing and the input that has been fed from the memory location of the MAC unit is 64-bit. The multiplier starts the computation process when the input has been given to it and the output obtained is 128-bit. Then the output of the multiplier has been given as input to the accumulator and adder block in the MAC unit architecture [6].

The Multiplier-Accumulator operation is represented by equation (1) respectively as follows:

$$F = \sum Pi\ Qi \quad (1)$$

The output of the adder and accumulator block is 129-bit i.e. one bit is carry (128-bit + 1bit) and then the output is feed back again to the same block of accumulator and adder [6].

VEDIC MULTIPLIER

Vedic multiplier is one such promising solution in today's world for wide range of applications because of its simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations [9]. The Vedic multiplier needs very less area as compared to other multiplier architecture. Hence the Vedic multiplier is faster than the array multiplier and booth multiplier. MAC always lies in the critical path that determines the speed of the overall hardware systems. Due to its regular and parallel structure it can be realized easily on silicon as well [10].

Urdhva-tiryakbhyam sutra

It is one of the best known techniques among the different types of Vedic sutras that are used in Vedic multiplier design. It is used to multiply two numbers together and it is also used in the division of a large number by another large number. The Vedic sutra shows how to handle multiplication of larger number (N×N bits) by breaking into smaller sizes. It is used in all numeric type of calculations and more commonly used in multiplication. It is used for computing any type of bit values and even uneven bit values and it reduces the complexity of the circuit, delay, power consumption, speed, etc. [5] The multiplication scheme can be explained by the following example as shown below in Figure-1.

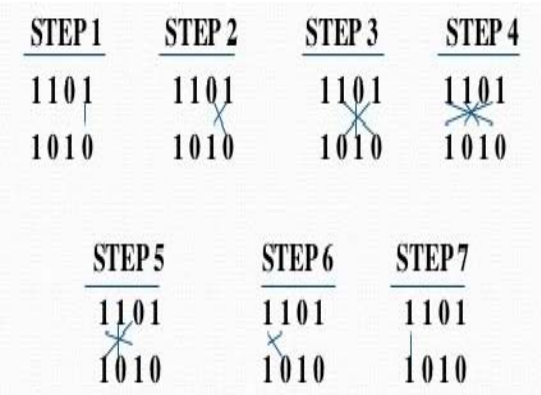

Figure-1. Example of U-T sutra [10].

EXISTING SYSTEM

Hence in this method the architecture of MAC unit is designed using different multipliers like Vedic multiplier, Dada multiplier, Braun multiplier and compared its performance with the Wallace multiplier. Therefore when compared to the Wallace multiplier, better performance and better results are obtained using other multiplier architectures.[6]

MAC unit

In general, MAC unit computes the product of two numbers and then adds that product to an accumulator register in which the input of MAC unit are obtained from the memory location and then given to the multiplier block. [6] Here the architecture of MAC unit consists of multiplier and adder- accumulator as shown below in Figure-2.

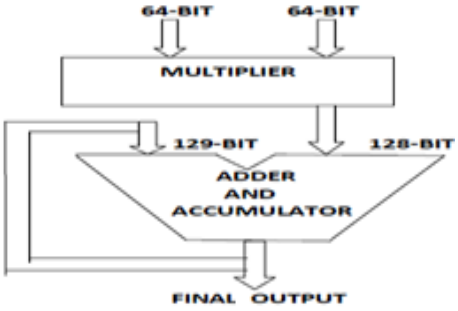

Figure-2. MAC unit architecture.

The MAC unit starts computation when the input has been given to it i.e., 64-bit and the output obtained is 128-bit. Then the output of the Vedic multiplier is given as input to the adder and accumulator block hence, the output obtained is 129-bit i.e. one bit is carry bit [6].

PROPOSED SYSTEM

The architecture of MAC unit (64-bit) is designed using modified Vedic multiplier and Adder-Accumulator block and Urdhva-tiryakbhyam principle is used to design the architecture of multiplier. Therefore compared to all other multiplier architecture, Vedic multiplier provides better performance and it is more efficient when it is implemented in MAC unit.

Proposed 1-bit full adder

Generally full adder is a single bit adder circuit in which it is like a half adder, but takes an additional input carry Ci. It is nothing but a combinational circuit that performs the arithmetic sum of three bits. Therefore full adder can also be constructed by cascading two half adders. Here the proposed full adder circuit used in the architecture of Vedic multiplier and in the Multiplier-Accumulator in the adder block is designed using double pass-transistor logic and transmission gate. To produce more realistic performance in the simulation, buffers are added to all the three input nodes and hence a transmission gate is added to the full adder circuit between the source and drain terminal which introduces wake-up time in the circuit. Wake-up time refers to "An act or instance of being awakened" such that it increases the time period which helps to speed - up the process of the adder design. Therefore the delay in the design further reduces and produces better results than the previous multiplier design. [11] The adder circuit is shown below in Figure-3 respectively as follows:

The proposed adder design reduces number of clock cycles in the circuit and by passing the circuit takes place which reduces the switching activities in the circuit. Hence the static and dynamic power consumption of the full adder design reduces to a great extent by means of obtaining both the outputs sum and carry in a single clock cycle.

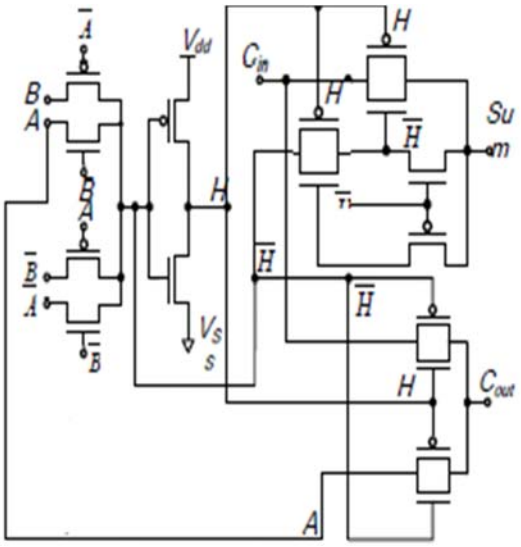

Figure-3. Proposed 1-bit full adder.

Proposed Vedic multiplier

The Vedic multiplier is more suitable for parallel processing and binary multiplication and hence in the architecture of multiplier a modified adder circuit is used by replacing the existing full adder circuit which in turn reduces the delay and provides better performance than the previous multiplier. The architecture of 64-bit Vedic multiplier is shown below in Figure-4 respectively as follows.

The Vedic multiplier operation is explained by means of the following example as, let us consider a two bit numbers where, the least significant bits are multiplied which gives the least significant bit of the final product (vertical) and the LSB of the multiplier is multiplied with the next higher order bit of the multiplicand (crosswise). Hence the sum is the third corresponding bit of the final product and the carry becomes the fourth corresponding bit of the final product. Therefore the process can be extended up to desired number of bits and it also can be applied uneven number of bits, etc.

Hence the proposed 64-bit MAC unit consists of 32-bit Vedic multiplier and 64-bit adder, in which the input given to the multiplier block is 64-bit and then the final output obtained is 128-bit.

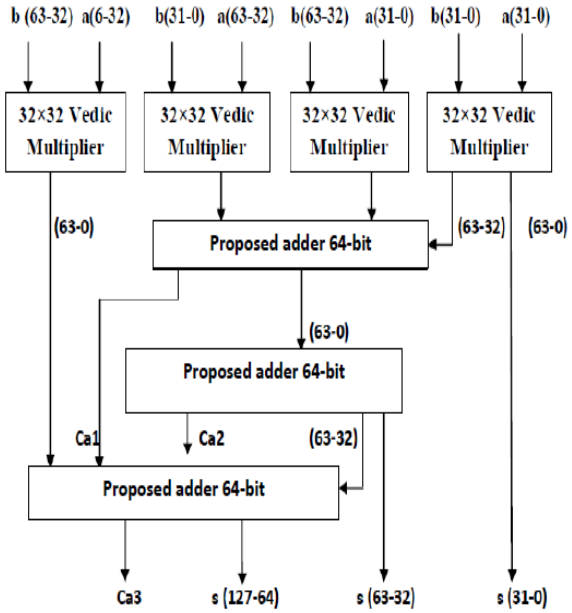

Figure-4. Proposed Vedic multiplier.

Proposed MAC unit

MAC unit is a combination of a multiplier implemented in combinational logic followed by an adder and an accumulator register which stores the result. The register output is given as feedback to the input of the adder block and on each clock cycle, the output of the multiplier is add-on to the register. Combinatorial multipliers require a large amount of logic, but can compute a product much quicker than the method of shifting and adding process. Digital signal processors were the first processors to be equipped with MAC, but now the technique is also common in general purpose processors [7]. Hence we proposed a modified MAC unit architecture which is of better efficiency, high speed, reduced power as shown in Figure-5, when compared to the existing MAC unit design.

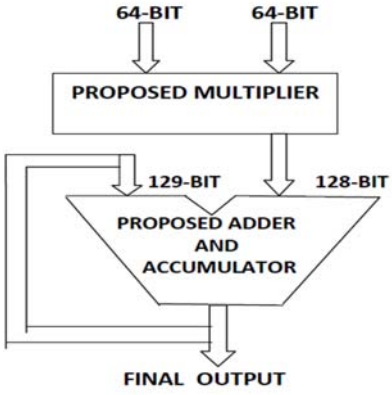

Figure-5. Architecture of proposed MAC unit.

RESULT ANALYSIS

The Proposed Multiplier-Accumulator design is analyzed using the tool XILINX ISE 13.2i by using Verilog-HDL and simulated using the MODEL SIM 6.3g and hence the performance of the multiplier is evaluated in which the power consumption of the circuit is reduced considerably when compared with the existing system. Then the performance of the MAC unit in the existing work which is constructed using Braun, Dadda, etc. is compared with different MAC units that are constructed previously. Therefore the performance of proposed MAC unit is compared with one which is constructed previously in existing system. The simulation results of the 64-bit proposed MAC unit and the Vedic multiplier is shown in Figures 6 and 7.

Figure-6 describes the simulation result of the Vedic multiplier using one bit full adder circuit output where clk, rst, x_in, y_in represents the inputs and p_out represents the output.

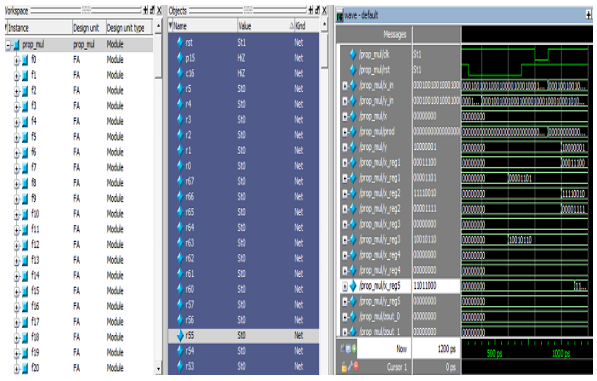

Figure-6. Simulation result of proposed Vedic multiplier.

Figure-7 describes the simulation result of the proposed MAC unit using the modified adder (proposed adder) output where clk, rst, enable, MAC_IN represents the inputs and MAC_TAP_OUT represents the output.

The simulation result of Proposed MAC unit is shown above in which, the input given to the Multiplier is 64-bit and it produces an output of 128 bit. Then, the output multiplier is given as input to the adder and accumulator block i.e., 128-bit. Hence the output of the MAC unit is 129 bit (128+1 bit) i.e., one bit is carry and it is again feedback to the adder and accumulator block as input.

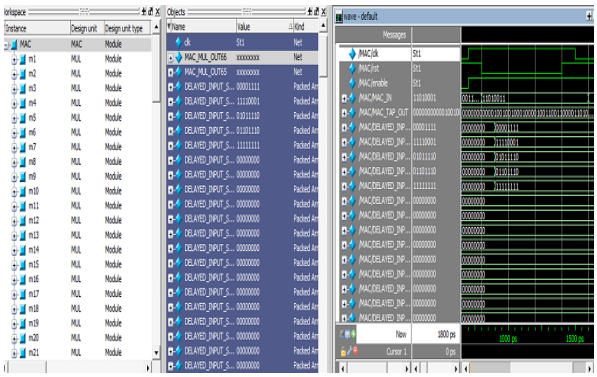

Figure-7. Simulation result of proposed MAC unit.

PERFORMANCE ANALYSIS

The existing and proposed MAC unit is simulated using QUARTUS II 9.0 and MODEL SIM 6.3g and numerical results has been obtained. Hence the Comparison of Average power for the Existing and proposed Multiplier-Accumulator are shown below in Table-1.

Table-1. Average power of Mac unit.

MAC unit	**Average power** (mW)
Existing System	88.27
Proposed System	73.22

Table-2 shows the comparison of the Logic delay and Route delay, etc., between the existing and proposed MAC unit.

Table-2. Delay of Mac unit.

S. No.	**Device**	**Logic delay** (ns)	**Route delay** (ns)	**Total delay** (ns)
1	Mac unit with RCA	84.725	61.745	146.470
2	Proposed Mac Unit	62.863	26.30	89.163

PERFORMANCE ANALYSIS CHART

The comparison of Average power between the existing and proposed MAC unit are shown below in Figure-8, respectively as follows:

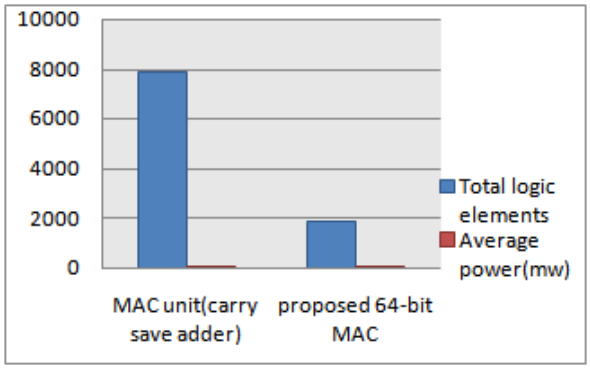

Figure-8. Comparison of average power between existing and proposed MAC unit.

Figure-9 shows the comparison of Existing and Proposed MAC unit using delay. Here the delay of the proposed MAC unit is reduced to a great extent when compared to the existing architecture of MAC unit and the performance analysis chart is shown below as follows:

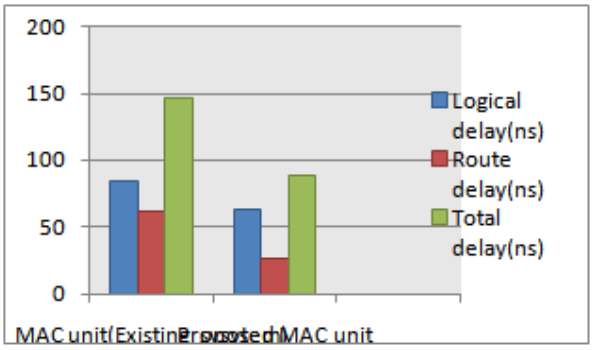

Figure-9. Performance analysis of MAC unit using delay.

CONCLUSIONS

Multiplier-Accumulator is thus designed using the new modified architecture of MAC unit and different parameters like delay, average power are determined. The proposed MAC unit is analyzed using Verilog-HDL by using Xilinx ISE 13.2i and simulated using MODELSIM 6.3g. As a result better performance can be achieved by reduction in delay and power of the proposed MAC unit than the previous architecture. Hence by using this modified architecture of MAC unit in most of the applications yields better results and better performance by reduction in power, delay and high speed.

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