VOL. 10, NO. 11, JUNE 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences
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PERFORMANCE ANALYSIS OF AN EFFICIENT TIME-TO-THRESHOLD PWM ARCHIECTURE USING CMOS TECHNOLOGY

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ABSTRACT

The CMOS active pixel sensors are used for reducing the pixel size and dynamic range of the sensors. Sensitivity is applicable in active pixel sensors. The photodiode is used for sensing element. The control circuit generates timing data, which is distributed in parallel to all pixels of array. In proposed system single event upset flip flop is used in 130 nm-technologies for better performance in average power. A conventional master-slave flip-flop is very sensitive to particular strike that causes single event upset. When the clock is low, single event upset is upset in the logic state of the slave latch, which results in the faulty output of flip-flop. The single event upset flip flop the proposed flip-flop achieves the smallest power delay product, which implies that the proposed flip-flop has better performance. High resolution in the mobile applications is done by CMOS active pixel sensors. CMOS image sensor used in medical applications for diagnostic capabilities like pills cam.

Keywords: CMOS image sensors (CIS), pulse width modulation (PWM), time-to-threshold conversion (TTC), active pixel sensor (APS), single event upset flip flop (SEU-FF).

INTRODUCTION

The Jet Propulsion Laboratory (JPL) developed CMOS active pixel sensor (APS) which is a second-generation solid state sensor technology. In the year of 1993 there is a wide need of CMOS active pixel sensors. The JPL has been the development of a "camera on a chip," which would have a full digital interface to the goal of the advanced imager technology effort. Highly integrated smaller and simpler electronics sensors will require the imaging instruments. Low power, low volume, delay product by using CMOS active pixel sensors technology, highly integrated imaging systems can be realized. A complete imaging system could require a power supply, a CMOS active pixel sensors imaging array with on-chip analog-to-digital converter (ADC) and a microprocessor is used to upload the instructions to the imager and downloads the image data also. In this mechanism, the pixels were designed in a 2Dimensional structure, with access enable wire shared by pixels in the same row, and output wire is shared by column. Rochass *et al*. (2005) proposed that each pixel did not have an amplifier, so an amplifier was connected at the end of each column. Some advantages of active pixel sensors are high sensitivity, low cost, high readout speed. With this CMOS technology due to the capability to build more pixels which results in more system-on-a-chip (SoC) integration.

A. Dickinson *et al* (2002) proposed that pixel array has on-chip timing, control, correlated double sampling and fixed pattern noise (FPN) suppression circuitry. The CMOS image sensors consists of passive pixel sensors and active pixel sensors .The CMOS active pixel sensors consists of array of pixels. Pixel sensors has an photo detector and three transistors an reset transistor, source follower or readout transistor and row select transistor. S. Kleinfelder *et al* (2002) proposed that the digital pixel sensors, each pixel consists of a photo detector, analog-to-converter(ADC), and a digital memory for temporary storage of data before the digital output signal is readout. Compare to the other pixel sensors like, PPS, APS, Photo gate APS, Pinned photodiode APS and DPS. In the present work Active pixel sensor is more efficient.

A latch can be to protect against single event upset. an single event upset latch is designed by adding additional transistors to its basic circuit structure such that the capacitance of sensitive nodes or the strength of sensitive transistors is increased. An single event upsetflip-flop can be built using such latches. For example, a triple path dual interlocked storage flip-flop uses two latches that interlock internal memory nodes to mitigate single event upsets. Namba *et al*. proposed a flip-flop that comprises various soft error latches to achieve single event upset tolerance and allow enhanced scan delay fault testing. A high performance single event upset flip-flop uses 12T storage cells and C-elements to mitigate single event upsets. An single event upset robust flip-flop is implemented based on two single event upset quatro cells. Single event upset flip-flop that has only one error detection circuit and one MUX, which introduces small area and performance overheads.

The enormous increase in market for image sensors explored in the last few years shows increase in sales and development of cameras. Imaging sensors are mainly classified into two types: 1.Complementary metal oxide semiconductor (CMOS) image sensors, 2.Charge couple device (CCD). Active pixel sensors (APS) are the emerging sensors for the replacement of existing and widely used charged couple device (CCD) sensors. Advancements in VLSI and other associated technologies has brought the digital cameras in use for applications like

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mobile digital photography, computer-based video, and in video digital cameras Now a days, APS are extensively used in webcams, robotics ,X-rays, computer based video toys, both still and video digital cameras.

EXISTING SYSTEM

The logical architecture for the time-to-threshold pulse width modulation imaging system is shown in Figure-1 it includes pulse width modulation pixel array, control circuits and time-to-threshold conversion. In M×N CIS array, a pixel P i,j is in readout mode when the row signal reset i is low and the row enable i is high. Timing waveforms of pixel integration including reset and enable phases, and time-to-threshold conversion based on row-by-row operation.

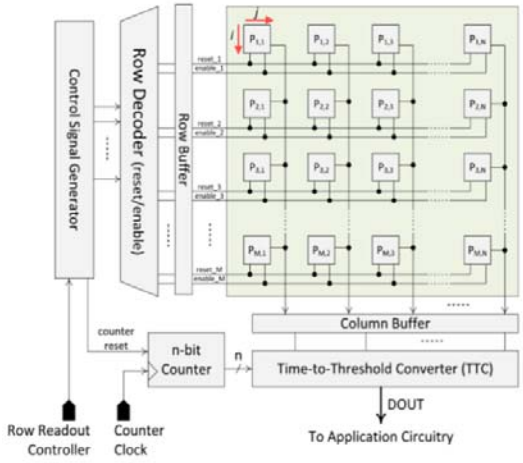

Figure-1. Time-to-threshold PWM architecture.

In this construct, A column line of the pulse width modulation readout is driven by digital form of a comparator having a higher drive current than a source follower of the 3T active pixel sensors. The digital form of output is compatible for asynchronous operation such as various self-resetting schemes .Whenever the accumulated signal reaches its threshold value the pulse width modulation is produced. Because the pulse modulation sensor acts as an Analog-to-Digital Converter, the architecture is highly suits for on-chip autonomous signal processing applications.

For image processing, an A/D circuitry converts pixel response to a digital value based on the incident illumination intensity. Various schemes of column-parallel A/D conversions such as delta-sigma, successive approximation, single slope, and cyclic ADCs are adopted in CIS to improve the frame rate.

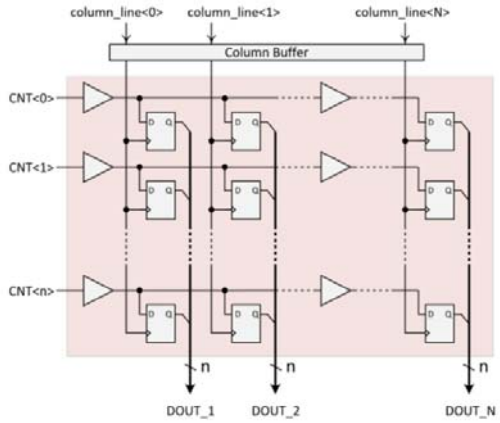

Figure-2. PWM pixel array.

In our architecture, a time-to-threshold conversion approach is implemented to obtain the digital value instead of the more conventional ADC-based techniques .For image processing, an A/D circuitry converts pixel response to a digital value based on the incident illumination intensity. Various schemes of column-parallel A/D conversions such as delta–sigma, successive approximation, single slope, and cyclic ADCs are adopted in CIS to improve the frame rate.

The counter in the VLSI architecture is synchronized with a rising edge of an enable signal. The output of the counter shown in Figure-2 is distributed for every N-bit register in the architecture. Pixel output signal column line is used as a clock signal for D flip-flops, which retain the output until the next column line is triggered. In our approach, the time-to-threshold conversion uses a 10-bit global counter and column-parallel registers. The area of the time-to-threshold conversion is estimated for over 10-megapixel-sized CIS and is compared with the reported conventional ADC schemes.

PROPOSED SYSTEM

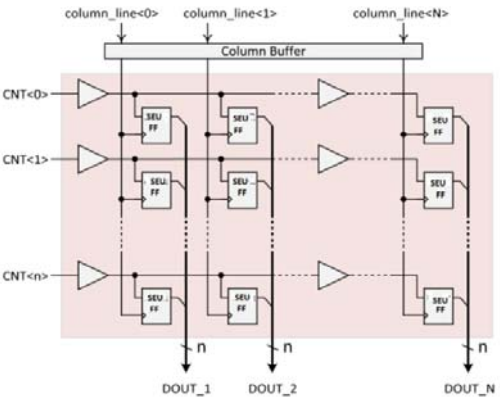

Figure-3. Proposed SEU flip flop.

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In proposed system single event upset flip flop is used in 130 nm-technologies for better performance in average power. A conventional master-slave flip-flop is very sensitive to particular strike that causes single event upset. When the clock is low, single event upset is upset in the logic state of the slave latch, which results in the faulty output of flip-flop. In this paper presents a single event upset flip-flop that can mitigate SEU with the error correction with the help of multiplexer that selects the correct value of the output signal. Using dynamic logic error correction is done when the SEU is in mater latch or slave latch when the clock is high or low.

When the clk is low, the NAND gate produces logic1. But when clk changes from low to high, the NAND gate produces logic 0 during this transition period. So PMOS M1 is turned on and NMOS M3 is turned off. Therefore, the signal S is precharged to logic 1 and this flip-flop outputs the value on node Q correctly via a MUX. After this rising edge the clock (clk), clk is high and the NAND gate output returns to logic 1. So PMOS M1 is off and NMOS M3 is on. The signal S remains at logic 1 to select the value on node Q as final output due to the open NMOS M2.

During the hold phase of the master latch (i.e., when clk is high), the transmission gate T2 is on and hence an single event upseton nodeA1 or B1 may result in a faulty 0-to-1or1-to-0 transition on node A2 and accordingly an erroneous value on node Q. This upset can be detected by the XNOR gate, which produces logic 1 during this invalid transition period. For example, suppose that the correct value on node A2 is logic 1 and hence the XNOR gate produces logic 0.

Single event upset flip flop

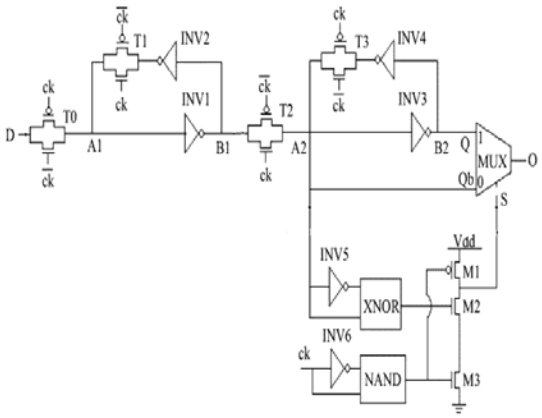

Figure-4. Single event upset flip flop.

when the correct value on node a2 is flipped to logic 0 by an single event upset in the master latch, the xnor gate will generate logic 1 during this invalid transition period. NMOS M2 is turned on, allows the current flow towards ground by the closed NMOS M3, then S is discharged to logic 0.

Therefore, the correct value on node Qb (rather than the erroneous value on node Q) is selected as the final output of this flip-flop when clk is high. When the clock (clk) is low, in slave latch the erroneous value will also be locked, but the signal S will remain at logic 0 to select the correct value on node Qb as the final output of this flip-flop. When clk is low, the NAND gate produces logic 1 and the XNOR gate produces logic0. So PMOSM1 and NMOSM2 are off and NMOS M3 is on. Suppose that no SINGLE EVENT UPSET occurs when clk is high. So the signal S remains at logic 1 to select the value on node Q as final output when clk is low.

However, during the hold phase of the slave latch (i.e. when clk is low), an single event upset may occur onnodea2orb2, resultinginafaulty0-to-1or1-to-0transition onnodea2andaccordinglyanerroneousvalueonnodeQ. This upset can be detected by the XNO Rgate, which produces logic1duringthisinvalidtransitionperiod.SoNMOSM2isturn edon and the signal S, is discharged to logic 0. Therefore, the correct value on node Qb (rather than the erroneous value on node Q) is selected as the final output of this flip-flop when clk is low.

Proposed single event up set flip flop

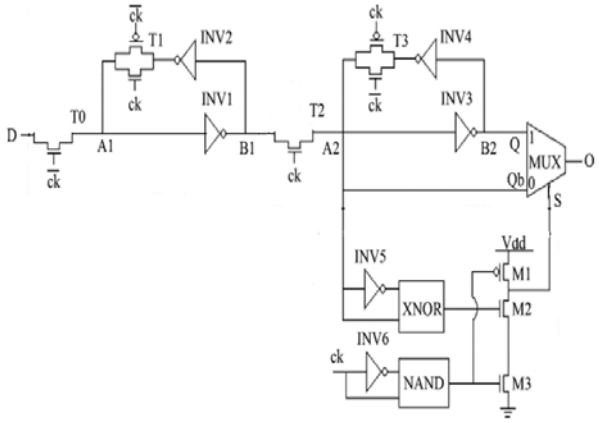

Figure-5. Proposed SEU flip flop.

In this single event upset flip flop the transmission gate is replaced by pass transistor, so that the given input T0 is pulsed by pass transistors and with the help of inverter INV1 it passes the correct value. When clock is low, the pass transistors switch to the other circuit and produce the erroneous output. When clock is high A1 is active and transmits the given value logic 0 which can be inverted. When the clock is low, single event upset is upset in the logic state of the slave latch, which results in the faulty output of flip-flop. In this paper presents an single event upset flip-flop that can mitigate SEU with the error correction with the help of multiplexer that selects the correct value of the output signal. Using dynamic logic

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error correction is done when the SEU is in mater latch or slave latch when the clock is high or low. According to the fault indication the multiplexer which is used in the SEU flip flop selects the correct signal to the final output.

The proposed flip-flop does not achieve the low power consumption, but the power value is smaller than the TPDICE flip-flop, firebird flip flop and Namba's flip flop. Among all the single event upset flip flop the proposed flip-flop achieves the smallest power delay product, which implies that the proposed flip-flop has better performance.

SIMULATION RESULTS

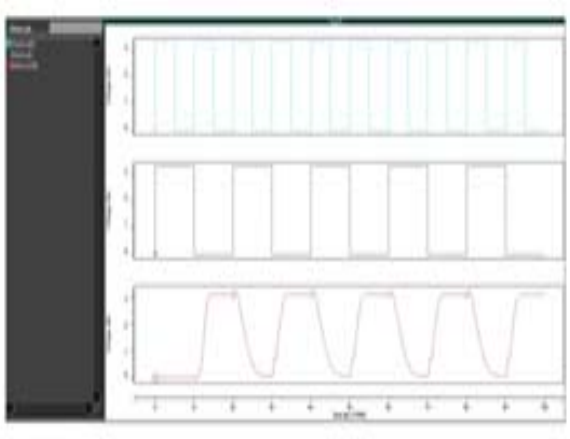

Figure-5. Single event upset flip flop output waveform.

1)V(25)→input,2)v(2)→clock,v(23)→output

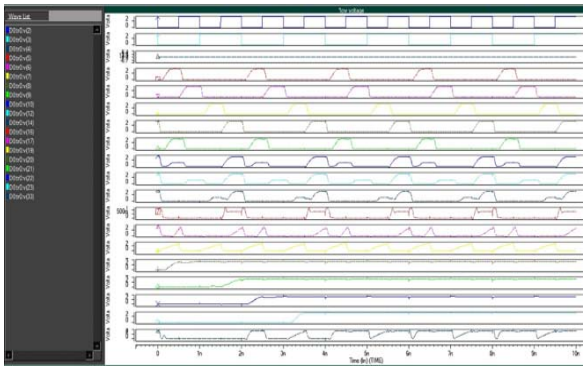

Figure-6. PWM single event upset simulation results.

1)V(3)→clock,2)v(2)→input1,3)v(10)→ input 2
4)V(23)→input3,5)v(9)→outpu1,6)v(11)→output
2,7)V(17)→output 3,8)v(32)→output4

PERFORMANCE ANALYSIS

Existing single event upset-FF

Single Event Upset-FF (Technology used: 130 nm-operating voltage: 3.3v-operating frequency: 1GHz**)**

Device	**Average power** (W)
Single event upset-FF	1.679e-04
Modified single event upset-FF	1.586e-04

In CMOS design, comparing the average power, the proposed SEU-FF is efficient than the existing SEU-FF.

Proposed single event upset-FF using PWM

Pulse Width Modulation (Technology used: 130nm-operating voltage: 3.3v-operating frequency: 1GHz).

Device	**Average power** (W)
Conventional PWM	8.679e-04
Single event upset-FF based PWM	6.397e-04
Modified single event upset based PWM	5.945e-04

In CMOS design, comparing the average power, the conventional PWM, proposed SEU-FF PWM is efficient than the existing SEU-FF based PWM.

CONCLUSIONS

The proposed time-to-threshold PWM VLSI architecture average power is reduced using standard 130-nm CMOS technology. This architecture provides different pulse widths that correspond to the level of luminance instead of the number of reset events when compared with TTFS approaches. Whenever the accumulated signal reaches its threshold value the pulse width modulation is produced. To detect faults the proposed flip-flop uses a dynamic logic based on error detection circuit by pre-charging and discharging operations. In CMOS design comparing the average power the conventional pulse width modulation, proposes single event upset flip floppulse width modulation is efficient than the existing single event upset-flip flop based pulse width modulation. According to the fault indication the multiplexer which is used in the SEU flip flop selects the correct signal to the final output. An efficient average power is reduced using modified single event upset flip flop. High resolutions in the mobile applications are done by CMOS active pixel sensors. CMOS image sensor used in medical applications for diagnostic capabilities like pills cam.

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