VOL. 10, NO. 12, JULY 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

PERFORMANCE ANALYSIS OF ARTIFICIAL NEURAL NETWORK USING LEAKAGE POWER REDUCTION TECHNIQUES FOR DSP APPLICATIONS

K. Gopika Rani, S. J. Jesanthe, N. Mathan and A. Nandhini
Department of Electronics and Communication Engineering, Sathyabama University, Chennai, India
E-Mail: gopikarani94@gmail.com

ABSTRACT

The statistics regarding the functionality of the brain was acquired tremendously. This leads to the birth of new technology called neural networks. A vast amount of information was processed in a human brain with the help of neurons. The interconnection between the neurons and the parallelism helps the brain to do the functions in few hundred milliseconds. The neural networks were able to solve the complex tasks. Unlike the traditional method, no explicit algorithm is required. In this paper, modified clocked CMOS D Flip Flop is taken and its parameters are analyzed for better performance by applying low power techniques. Then it is applied in the Artificial Neural Network (ANN) to provide an improved way for computing mathematical functions. It concludes that all the low power techniques reduce the leakage power comparatively. This resultant ANN architecture can be applied for low power digital applications.

Keywords: artificial neural network, leakage power, DSP, parallelism, mC^{2}MOS D flip-flop.

1. INTRODUCTION

Nervous cells, or neurons, are excitable cells specialized in receiving and sending electrical and chemical impulses. The nucleus controls the impulses originating from other neurons and generates a response. This behavior can be mimicked by a computer, thus originating in a simplified neuron which is known as an artificial neuron. Artificial Neural Networks (ANN) are composed of these artificial neurons, usually disposed in layers and connected so as to form networks [6]. Various problems in the field of pattern recognition, image processing and medical diagnostic etc. can be resolved by Artificial Neural Network (ANNs). The biologically inspired ANNs are parallel and distributed information processing systems [20].

A most important feature of Artificial Neural Networks (ANN) is their learning ability. Size and real-time considerations show that on-chip learning is necessary for a large range of applications [8], [3]. In contrast to software implementation of ANN, hardware implementation provides a high level of parallelism. This allows us to make several computations concurrently in order to have a higher processing speed [8], [10], [11], [12]. In addition, the hardware implementation is highly portable since it has minimum requirements in area and power consumption, and provides standalone [8]. Nowadays the development of intelligent and more natural advanced devices, without need of knowledge for parameters setting activity, is inspiring the research groups worldwide. The need to have learning and adaptive capacity for such smart devices can be satisfied using neural networks hardware and software implementation [3]. Thus this paper aims to help the readers to identify the bridges in learning about the artificial neural network.

2. MODIFIED CLOCKED CMOS D-FLIP FLOP

The schematic of mC^{2}MOS D flip-flop is shown in Figure-1 is one of the resilient classical structures. The mC^{2}MOS is robust to clock slope variation due to the local clock buffering. The other classical structures have fast pull-up by using complementary pass gates which reduces its robust. Therefore mC^{2}Mos flip flop is used to have high durability.

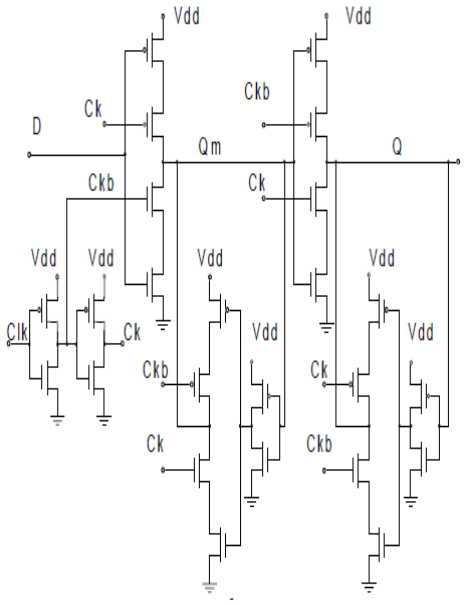

Figure-1. mC^{2}MOS D-Flip Flop.
(Source ref [22])

The mC^{2}MOS circuit shows the minimum energy degradation and its mean energy increases up to 50%. Its main advantage is working in high performance and low power processors.Compared to conventional D-Flip Flops, mC^{2}MOS D flip-flop having less number of transistors [22]. Modified clocked CMOS D Flip Flop has a special character involving the clock pulse. In this circuit, two inverters are used to obtain a most reliable input clock pulse. The original clock pulse (clk) is first inverted to get the negative clock pulse (ckb) and is further inverted to obtain the reliable positive clock pulse (ck).

3. ARTIFICIAL NEURAL NETWORK

Artificial neural networks (ANN) have found widespread deployment in a broad spectrum of classification, perception, association and control applications. Any kind of standard data can be categorized by using the hardware implementation.

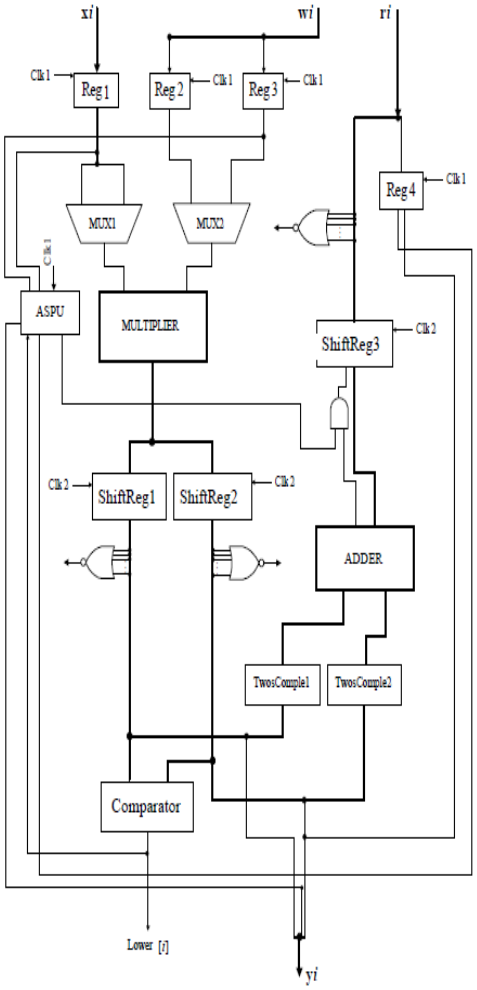

Figure-2. Artificial neural network.
(Source ref [18])

Artificial neural networks (ANNs) have been mostly implemented in software [12]. Because implementing in software helps in detecting and recovering the errors made in the architecture. Since software implementation has many advantages such as less complexity, low cost and it reduces the time for implementing. It includes many basic logic gates and basic digital circuits as shown in Figure-2. All these circuits have been designed using 130nm CMOS technology. It can be used for performing any mathematical operation in a simple manner.

4. LOW POWER TECHNIQUES

Complementary Metal Oxide Semiconductor (CMOS) is a major technology in Very Large Scale Integration (VLSI) circuit design in case of power consumption. Power consumption is the major problem in the real world applications such as mobile applications. There is a common approach for the reduction of power consumption in any digital design using low power techniques.

Some of the low power techniques used in this paper is

a) Full Sleep Approach

b) Sleepy Keeper Approach

c) Leakage Feedback Approach

a) Full Sleep approach

Sleep approach in Figure-3 is the most classical than other approaches. Basically, in sleep approach other than the pull-up and pull-down network an extra pMOS and nMOS is connected to the network. More particularly, pMOS is connected between Vdd and the pull-up network and nMOS is connected between the pull-down network and ground. During the active mode the sleep transistors are turned on and during the sleep mode it is turned off. While the sleep transistors are in off condition, it cuts off the power source for the network. This effectively reduces the leakage power generated in the network [1].

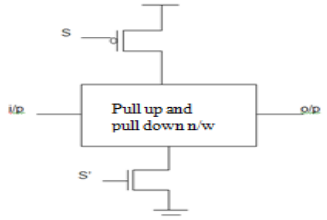

Figure-3. Full Sleep approach.

b) Sleepy Keeper approach

Sleepy Keeper in Figure-4 is one of the most efficient techniques used for reducing the leakage power. In this approach, parallel pMOS and nMOS transistors are

linked to the pull-up and pull-down network. These combinations of pMOS and nMOS transistors are connected between Vdd and the pull-up network and also between the pull-down network and ground. The gate terminal of nMOS placed between Vdd and the pull-up network is connected to the gate terminal of pMOS placed between the pull-down network and ground. This helps to maintain the proper logic of the circuit and reduces the leakage power efficiently [1].

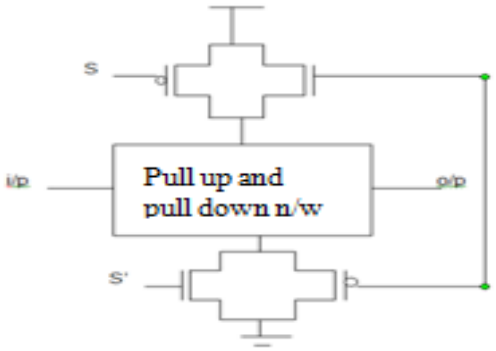

Figure-4. Sleepy Keeper approach.

c) Leakage feedback approach

Another method for reducing the power consumption is leakage feedback approach. In this approach, two parallel connected pMOS are placed between Vdd and the pull-up network as shown in Figure-5. Similarly, two parallel connected nMOS are placed between the pull-down network and ground. In this method, the inversion of the output signal is taken and is given as a feedback to the pMOS and nMOS chained with the pull-up and pull-down network respectively. This maintains the proper logic of the circuit during stand-by mode. This approach most commonly increases the overall performance of the circuit. [1]

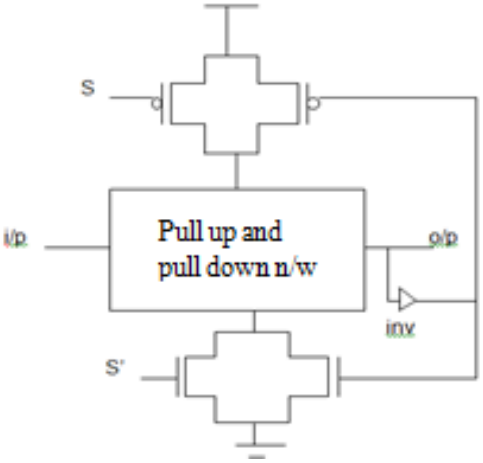

Figure-5. Leakage Feedback approach.

These leakage power reduction techniques have been applied in the existing mC^{2}MOS D flip flop. The resulting flip flop with low power has been further applied in ANN. The performance and comparison of parameters have been examined below.

5. SIMULATION RESULTS

5.1 Existing mC^{2}MOS D Flip Flop

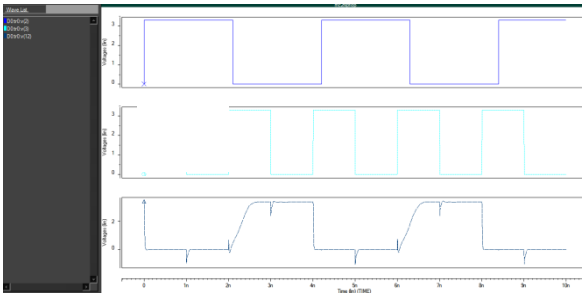

Figure-6. Existing mC^{2}MOS D Flip Flop output.

The above Figure-6 represents the input signal, clock pulse and output waveform of mC^{2}MOS DFF taken in the nodes 2, 17, 12 respectively.

5.2 Existing artificial neural network

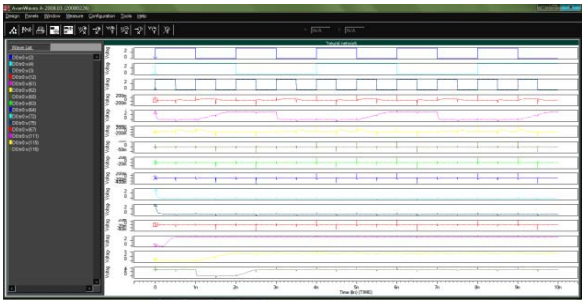

Figure-7. Existing Artificial Neural Network output.

The Figure-7 denotes the input and output waveforms at node 2 and 116 respectively. The remaining waveforms are intermediate outputs of multiplexer, shift register, etc.

5.3 Proposed mC^{2}MOS D Flip Flop using full sleep approach output

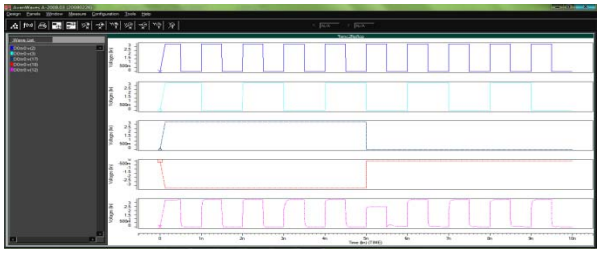

Figure-8. Proposed mC^{2}MOS D- Flip Flop Using Full Sleep Approach Output.

The Figure-8 explains the modification in the output of mC^{2}MOS DFF after applying the full sleep pulse in node 17 and 18.

5.4 Proposed mC^{2}MOS D Flip Flop using sleepy keeper approach output

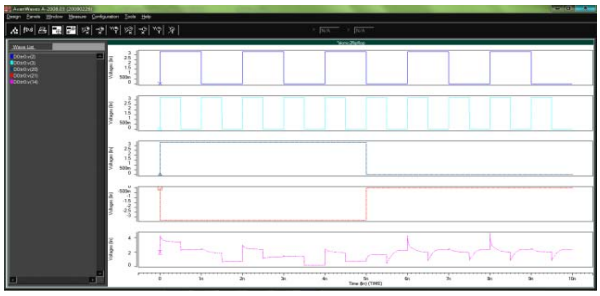

Figure-9. Proposed mC^{2}MOS D- Flip Flop using sleepy keeper approach.

The Figure-9 points out the modification in the output of mC^{2}MOS DFF using sleepy keeper technique by applying the sleep and sleepbar pulse in node 20 and 21 respectively.

5.5 Proposed mC^{2}MOS D Flip Flop using leakage feedback approach output

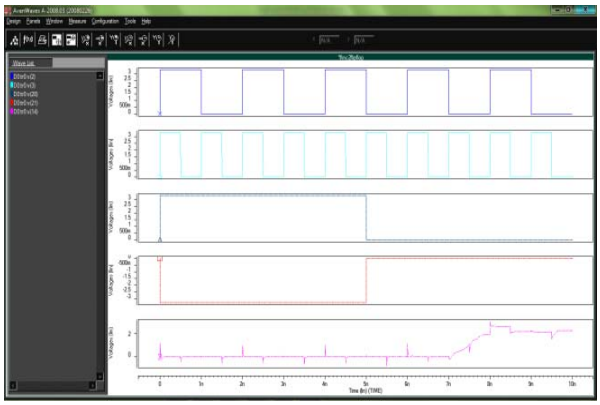

Figure-10. Proposed mC^{2}MOS D- Flip Flop using leakage feedback approach.

The Figure-10 shows the modification in the output of mC^{2}MOS DFF along with the negative feedback using leakage feedback technique by applying the sleep and sleepbar pulse in node 20 and 21 respectively.

5.6 Proposed artificial neural network using full sleep approach output

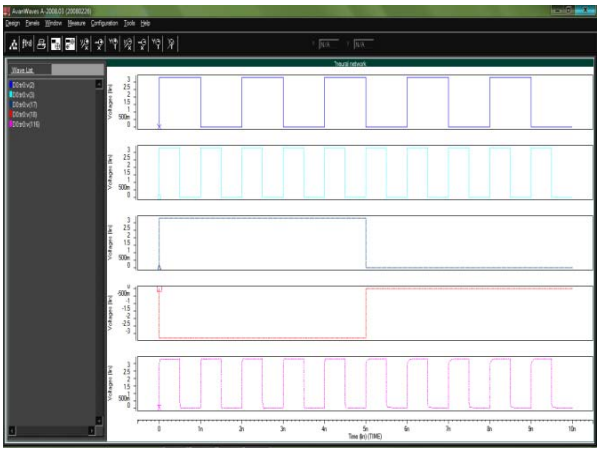

Figure-11. Proposed mC^{2}MOS D- Flip Flop Using Full Sleep Approach Output.

The Figure-11 briefs the output of ANN with modified mC^{2}MOS DFF using full sleep approach. Here, the output is measured at the node 116.

5.7 ANN with proposed mC^{2}MOS D Flip Flop using sleepy keeper approach output

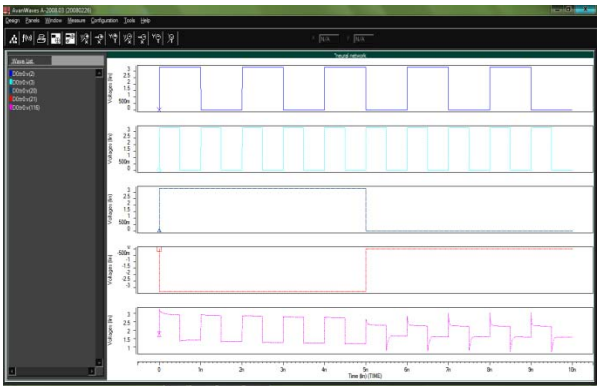

Figure-12. Proposed mC^{2}MOS D- Flip Flop Using Sleepy Keeper Approach.

The Figure-12 describes the output of ANN at node 116 with modified mC^{2}MOS DFF using sleepy keeper technique.

5.8 ANN with proposed mC^{2}MOS D Flip Flop using leakage feedback approach output

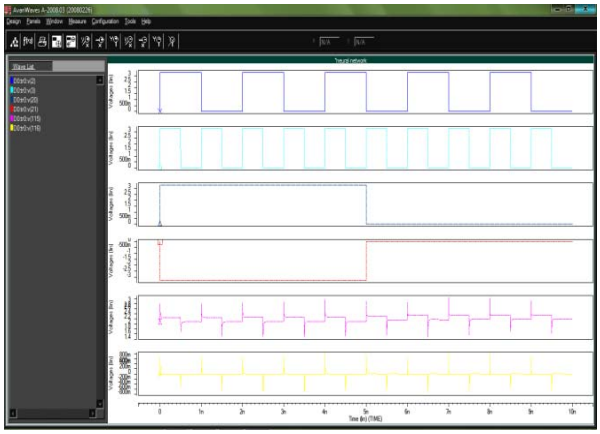

Figure-13. Proposed mC^{2}MOS D- Flip Flop using leakage feedback approach.

The Figure-13 gives the ANN output at node 116 after modifying mC^{2}MOS DFF using leakage feedback method.

Here, HSPICE tool is used for performing the simulation process all the digital circuits involved in the ANN architecture.

6. PERFORMANCE ANALYSIS

Table-1. Comparison of existing and proposed mC^{2}MOS D-FF in 130nm CMOS technology.

Low power techniques	**Power** (W)	**Delay** (s)	**Power delay product** (J)
Existing	96.89 µ	712.69 p	69.012 f
Full Sleep	17.06 µ	615.28 p	10.496 f
Leakage Feedback	22.31 µ	541 p	12.0697 f
Sleepy Keeper	7.935 µ	499.56 p	3.964 f

The above table explains the power reduction in the flip flop with leakage power reduction techniques than the existing flip flop.

Table-2. Comparison of existing and proposed artificial neural network in 130nm CMOS technology.

Low power techniques	**Power** (W)	**Delay** (s)	**Power delay product** (J)
Existing	1.972 m	110.55 p	218.82 f
Full Sleep	0.6586 m	71.88 f	47.34 a
Leakage Feedback	0.8516 m	38.024 p	32.38 f
Sleepy Keeper	0.5049 m	34.767 f	18.56 a

The above table explains the power reduction in the ANN with modified flip flop than the existing ANN.

CONCLUSIONS

In this paper, the circuits were designed using 130nm CMOS technology. The circuits performance parameters power, delay and power delay product were compared. The simulation for 130nm MOSFET was carried out at 3.3 V. The transient, power, delay and power delay product analyses have been carried out. These observations are compared. It is noted that, the proposed circuits in 130nm MOSFET consumes less power than the existing circuits. The modified Clocked Complementary Metal Oxide Semiconductor (mC^{2}MOS) D Flip Flop is designed using low power techniques like sleep approach, sleepy keeper approach and leakage feedback approach in 130nm CMOS technology. The result shows that the sleepy keeper technique is maintaining the output properly during ideal mode and reduces the power leakage effectively than other approaches.

REFERENCES

[1] Ajay Kumar Dadoria and Kavita Khare. 2014. A novel approach for leakage power reduction techniques in 65nm technologies. International Journal of VLSI design and Communication Systems (VLSICS). 5(3).

[2] Avogadro. M, M. Bera, G. Danese, F. Leporati, A. Spelgatti. 2004. The Totem neurochip: an fpga implementation. Proceedings of fourth IEEE International Signal Processing and Information Technology. pp. 461-464.

[3] Batsukh Batbayar. 2008. Improving time efficiency of feed forward Neural Network learning. pp. 97-99.

[4] Beuchat. J.L, J. O. Haenni, E. Sanchez. 1998. Hardware reconfigurable neural networks, IPPS,

SPDP workshops. pp. 91-98, url=citeseer.ist.psu.edu/beuchat98 hardware.html.

[5] Bridges. S, M. Figueroa, D. Hsu, C. Diorio. 2005. A reconfigurable vlsi learning array. Proceedings of the 31st European Solid-State Circuit Conference. pp. 117-120.

[6] Diego Santos, Henrique Nunes, Fernando Morgado-Dias. 2012. Dual-processor neural network implementation in FPGA. 10th Portuguese Conference on Automatic Control.

[7] Esraa Zeki Mohammed and Haitham Kareem Ali. 2013. Hardware Implementation of Artificial Neural Network Using Field Programmable Gate Array. International Journal of Computer Theory and Engineering. 5(5).

[8] Félix Moreno, Jaime Alarcón, Rubén Salvador and Teresa Riesgo. 2008. FPGA Implementation of an Image Recognition System based on Tiny Neural Networks and on-line Reconfiguration. IEEE explores.

[9] Figueiredo. M.A, C. Gloster. 1998. Implementation of a probabilistic neural network for multi-spectral image classification on an fpga based custom computing machine. Proceedings. Vth Brazilian Symposium on Neural Networks. pp. 174-178.

[10] Hammerstrom. B. 1990. A vlsi architecture for high-performance, low cost, on-chip learning. IJCNN International Conference on Neural Network. 2: 537-544.

[11] Hanaa T. El-Madany, Faten H. Fahmy, Ninet M. A. El-Rahman and Hassen T. Dorrah. The Online Journal on Electronics and Electrical Engineering (OJEEE). 4(1): Ref. no.: W11-0083, pp. 495-501.

[12] Hikawa H. 1995. Implementation of simplified multilayer neural networks with on-chip learning. Proceedings IEEE International Conferences on Neural Networks. 4: 1633-1637.

[13] Krasteva. Y.E, E. de la Torre, T. Riesgo. 2006. Partial reconfiguration for core relocation and flexible communications. Proceedings of Reconfigurable Communication-centric SoC. pp. 91-97, Montpellier.

[14] Mathan. N. 2014. CNTFET based Highly Durable Radix-4 Multiplier using an efficient Hybrid Adder. Biosciences Biotechnology Research Asia. 11(3): 1855-1860.

[15] Murata. N, S. Yoshizawa and S. Amari. 1993. Learning curves, model selection and complexity of neural networks,‖ in Advances in Neural Information Processing Systems 5, S. Jose Hanson, J. D. Cowan, and C. Lee Giles, ed. San Mateo, CA: Morgan Kaufmann, 1993, pp. 607-614.

[16] Pino.B, F. J. Pelayo, J. Ortega, A. Prieto. 1999. Design and evaluation of a reconfigurable digital architecture for self-organizing maps, Proceedings, Int. Conf. Microelectronics for neural, fuzzy and bioinpired system. pp. 395-402.

[17] Robert Lange. Design of a generic neural network FPGA-Implementation with Entwicklung einer generischen FPGA-Implementierung Neuronaler Netze

[18] Rodrigo martins da silva, nadia nedjah, luiza de macedo mourelle. 2011. Compact yet efficient hardware architecture for multilayer-perceptron neural networks. Revised control and automatic. 22(6): 647-663.

[19] Starzyk. J.A, Z. Zhen, L. Tsun-Ho. 2005. Self-organizing learning array. IEEE Transactions on Neural Networks. 16: 355-363.

[20] Suhap Sahin, Yasar Becerikli and Suleyman Yazici. 2006. Neural Network Implementation in Hardware Using FPGAs. I. King *et al*. (Eds.): ICONIP, Part III, LNCS 4234, pp. 1105.

[21] Vitabile S, A. Gentile, G. B. Dammone, F. Sorbello. 2003. Multi-layer perceptron mapping on simd architecture. Proceedings of the 12th IEEE workshop on Neural Networks for signal processing. pp. 667-675.

[22] Vladimir Stojanovic, Vojin Oklobdzija and Raminder Bajwa. Comparative Analysis of Latches and Flip-Flops for High-Performance Systems.

[23] Xiaobin.M, J. Lianwen, S. Dongsheng, Y. Junxun. 2003. A mixed parallel neural networks computing unit implemented in fpga, IEEE Int. Conf. Neural Networks and Signal Processing, Nanjing, China.

[24] Yun. S.B, Y. J. Kim, S. S. Dong, C. H. Lee. 2002. Hardware implementation of neural network with expandible and reconfigurable architecture. Proceedings, IEEE Int. Conf. on neural information. 2: 970-975.