VOL. 10, NO. 12, JULY 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

ASSESMENT OF EQUAL AND UNEQUAL AMPLITUDE CARRIERS FOR A SINGLE PHASE FIVE LEVEL DIODE CLAMPED INVERTER

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ABSTRACT

This work presents the comparison of various Pulse Width Modulation (PWM) techniques for the chosen single phase half bridge DCMLI (Diode Clamped Multi Level Inverter). In this paper, a single phase half bridge diode clamped multilevel inverter is simulated with sinusoidal, THI (Third Harmonic Injection), Trapezoidal, TAR (Trapezoidal Amalgamated Reference) and Stepped Wave reference with Equal Amplitude Carriers (EAC) and UEAC (Un Equal Amplitude Carriers). The proposed EAC and UEAC is applied for various PWM strategies like PD (Phase Disposition) PWM, POD (Phase Opposition and Disposition)PWM, APOD (Alternative Phase Opposition and Disposition) PWM, CO (Carrier Overlapping)PWM, PS(Phase Shift), PWM and VF(Variable Frequency) PWM with EAC and UEAC. For all the PWM methods and references the UEAC produces less THD and higher fundamental RMS (Root Mean Square) values except for m_a =1. For m_a =1 the EAC provides less THD (Total Harmonic Distortion) and higher fundamental RMS (Root Mean Square) values for all the PWM methods and references. The simulations are carried out through Power System Block Set/MATLAB/SIMULINK.

Keywords: amplitude carriers, DCMLI (Diode clamped multi level inverter), advanced references, sinusoidal, R-Load, THD.

INTRODUCTION

The power electronics device which converts DC input voltage to AC output voltage at required voltage and frequency level is known as inverter. The AC output voltage could be of fixed or variable magnitude at fixed or variable frequency. Inverters can be broadly classified into two level inverter and Multi Level Inverter (MLI). An inverter topology for high voltage and high power applications that seems to be gaining interest is the MLI. The main feature of the MLI is its ability to reduce the voltage stress on each power device due to the utilization of multiple levels on the DC bus. MLIs as compared to two level inverters have advantages like minimum harmonic distortion, reduced Electro Magnetic Interference/Radio Frequency Interference (EMI/RFI) and operation at several voltage levels. MLIs are being utilized for multi-purpose applications such as active power filters, static VAR compensators etc. MLI includes an array of power semiconductors and capacitor/voltage sources. The output of MLI is voltage with stepped waveform. Bhagwat*et al.* [1] suggested a generalized structure of a multilevel voltage source thyristor inverter is proposed. The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. A simple uniform PWM control of the output voltage is seen to be sufficient to practically remove all remaining harmonics. Harmonic analysis of n-step waveform is given, and the experimental results obtained on a three-step inverter are presented. Menzies *et al* [2] developed large induction motor drives with low torque ripple and fast dynamic response for new or retrofit applications has been limited by the device ratings and problems of series connections. This paper investigates the use of a five-level GTO voltage-sourced inverter for large induction motor drives. The advantages of such a drive are that single GTO thyristor may be used at each level, thereby avoiding the need for series connection of the thyristor. The thyristor are well protected from overvoltages by the clamping action of the DC supply capacitors. The disadvantages are that each DC level requires a separate supply, four in the case of the five-level inverter, and that the devices are not equally loaded. This paper reviews the basic operation of the five-level inverter and possible PWM voltage/frequency control techniques for the specific application of induction motor drives. The simulation results clearly show the unequal loading of the devices and the need for independent voltage supplies for the five levels. It is shown that a combination of several PWM techniques offers the best solution for the drives application. The conclusions indicate that large induction motors with ratings up to 22 MVA, 7.46 kV may be supplied by the five-level inverter using available 4.5 kV, 3.0 kA GTO thyristor. The recommended supply for such an inverter with full regenerative operation over the complete speed range is four, four-quadrant converters in a quasi-24-pulse configuration. Low in [3] describes the closed-loop control of a single-phase pulse width modulated (PWM) inverter using the generalized predictive control (GPC) algorithm. This approach determines the desired switching signals by minimizing a

cost function that reduces the tracking error and the control signals. Experimental results have demonstrated that the prototype system performs well. Yuan *et al* [4] explores the spontaneous coupled clamping-capacitor-current control loops and the resultant self-balancing property of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter. The case of the three-level capacitor-clamping-inverter under sub-harmonic PWM modulation is dealt with first. The case of the multilevel capacitor-clamping-inverter (M>3) under sub-harmonic PWM modulation is then analysed. Test results on a half-bridge three-level capacitor-clamping-inverter prototype under sub-harmonic PWM modulation are demonstrated. Corzineand Familiant [5] discussed original practical and theoretical results (lambda =1.523 mu m) for both optimal and suboptimal detection of digital PPM. When operating with 16 slots of 20 ns duration, the sensitivity was measured to be -46.6 dBm for optimal detection, and -45.9 dBm for suboptimal detection. It is concluded that suboptimal filtering significantly reduces receiver complexity, and results in degradation in sensitivity of only 0.7 dB. Chiasson [6] proposed the method to eliminate harmonics in a switching converter is considered. That is, given a desired fundamental output voltage, the problem is to find the switching times (angles) that produce the fundamental while not generating specifically chosen harmonics. In contrast to the well known work of Patel and Hoft and others, here all possible solutions to the problem are found. This is done by first converting the transcendental equations that specify the harmonic elimination problem into an equivalent set of polynomial equations. Then, using the mathematical theory of resultants, all solutions to this equivalent problem can be found. In particular, it is shown that there are new solutions that have not been previously reported in the literature. The complete solutions for both unipolar and bipolar switching patterns to eliminate the fifth and seventh harmonics are given. Finally, the unipolar case is again considered where the fifth, seventh, 11th, and 13th harmonics are eliminated along with corroborative experimental results. Juanand Moran [7] focussed on minimizing the number of power supplies and semiconductors for a given number of levels. Multilevel inverters with a large number of steps (more than 50 levels) can generate high quality voltage waveforms, good enough to be considered as suitable voltage template generators. Many levels or steps can follow a voltage reference with accuracy, and with the advantage that the generated voltage can be modulated in amplitude instead of pulse-width modulation. The main disadvantage of this type of topology is the large number of power supplies and semiconductors required to obtain these multistep voltage waveforms. Different combinations of topologies are presented, and the corresponding mathematical relations have been derived. This paper shows optimized curves to obtain the relation between a minimum number of power semiconductors required for a given number of levels. Experimental results obtained from an optimized prototype, capable of generating 81 levels of voltage with only four power supplies and 16 transistors per phase, are shown. Wells *et al* [8] suggested calculating easily and quickly the desired waveform without solution of coupled transcendental equations. A modulation-based method for generating pulse waveforms with selective harmonic elimination is proposed. Harmonic elimination, traditionally digital, is shown to be achievable by comparison of a sine wave with modified triangle carrier. Urmila and Subbarayudu [9] presents a comparative study of nine level diode clamped inverter for constant Switching frequency of sinusoidal Pulse width Modulation and sinusoidal Natural Pulse width Modulation with switching frequency Optimal Modulation. The multilevel inverter topology gives the advantages of usage in high power and high voltage application with reduced harmonic distortion without a transformer. Khoucha*et al* [10] presents the comparison study for a cascaded H-bridge multilevel direct torque control (DTC) induction motor drive. Earlier studies have pointed out the limitations of conventional inverters, especially in high-voltage and high-power applications. In recent years, multilevel inverters are becoming increasingly popular for high-power applications due to their improved harmonic profile and increased power ratings. Several studies have been reported in the literature on multilevel inverters topologies, control techniques, and applications. However, there are few studies that actually discuss or evaluate the performance of induction motor drives associated with three-phase multilevel inverter. In this case, symmetrical and asymmetrical arrangements of five- and seven-level H-bridge inverters are compared in order to find an optimum arrangement with lower switching losses and optimized output voltage quality. The carried out experiments show that an asymmetrical configuration provides nearly sinusoidal voltages with very low distortion, using less switching devices. Moreover, torque ripples are greatly reduced. Nami*et al* [11] proposed a comparative study has been carried out to present high performance of the proposed configuration to approach a very low total harmonic distortion of voltage and current, which leads to the possible elimination of the output filter. A novel H-bridge multilevel pulse width modulation converter topology based on a series connection of a high-voltage diode-clamped inverter and a low-voltage conventional inverter is proposed in this paper. A dc link voltage arrangement for the new hybrid and asymmetric solution is presented to have a maximum number of output voltage levels by preserving the adjacent switching vectors between voltage levels. Hence, a 15-level hybrid converter can be attained with a minimum number of power components. Regarding the proposed configuration, a new cascade inverter is verified by cascading an asymmetrical diode-clamped inverter, in which 19 levels can be synthesized in output voltage with the same number of components. To balance the dc link capacitor voltages for

the maximum output voltage resolution as well as synthesize asymmetrical dc link combination, a new multi-output boost converter is utilized at the dc link voltage of a seven-level H-bridge diode-clamped inverter. Simulation and hardware results based on different modulations are presented to confirm the validity of the proposed approach to achieve a high-quality output voltage. Kangarlu*et al* [12, 13] proposes a new topology based on the non-insulated dc voltage sources for multilevel inverter with reduced number of switching devices. Multilevel inverters have an important portion in power processing in power systems. These inverters have some inherent advantages such as ability to operate with high power and voltage, improved output waveform quality and flexibility which make them attractive and more popular. As a result, it reduces control complexity and gate driver circuits. The proposed topology is a general topology which can be easily extended to a desired number of voltage levels. All of the desired output voltage levels (both odd and even) can be achieved using the proposed topology. The validity of the proposed multilevel inverter is verified with both computer simulation and experimental results from a 15-level laboratory prototype. Babaei*et al* [14, 15] developed a new general cascaded multilevel inverter using H-bridges is proposed. The proposed topology requires a lesser number of dc voltage sources and power switches and consists of lower blocking voltage on switches, which results in decreased complexity and total cost of the inverter. These abilities obtained within comparing the proposed topology with the conventional topologies from aforementioned points of view. Moreover, a new algorithm to determine the magnitude of dc voltage sources is proposed. The performance and functional accuracy of the proposed topology using the new algorithm in generating all voltage levels for a 31-level inverter are confirmed by simulation. This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI employing Sinusoidal, THI and 60 degree references for different PWM switching strategies. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

MULTILEVEL INVERTER

Multilevel inverter as compared to two level inverters have advantages like minimum harmonic distortion, reduced EMI/RFI generation and operation on several voltage levels. A multi-stage inverter is being utilized for multi-purpose applications such as active power filters, static VAR compensators and electric utility application etc. Over the past two decades, MLIs have attracted wide interest both in the scientific community and in the industry. The reason for the increased interest is that the MLIs are a viable technology in high power applications. Power conditioning systems are often designed to supply an AC load from DC source. An inverter should provide constant and ripple free AC voltage to ensure the safety of the equipments. Diode clamped multilevel inverter is a very general and widely used topology. DCMLI works on the concept of using diodes to limit voltage stress on power devices. A DCMLI producing m levels on the output voltage consists of (m-1) capacitors on the DC bus. Figure-1 shows a single phase half-bridge five level diode clamped inverter. The order of numbering of the switches is S1, S2, S3, S4, S1', S2', S3' and S4'. The DC bus consists of four capacitors C1, C2, C3 and C4 acting as voltage divider. For a DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$ and voltage stress on each device is limited to $V_{dc}/4$ through clamping diode. The middle point of the four capacitors 'n' can be defined as the neutral point (mid point).

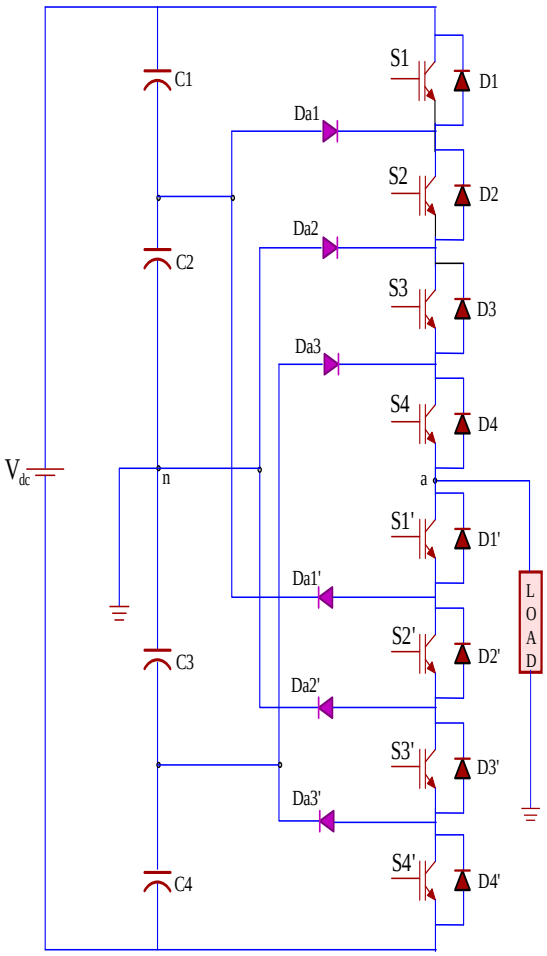

Figure-1. Half bridge five level diode clamped inverter.

MODULATION STRATEGIES

Several CFDs exist in multi-carrier PWM strategies for MLIs. These strategies have more than one carrier option that can be triangular, saw tooth, a new function etc. As far as the particular carrier signals are concerned, there are multiple CFDs including function, frequency, amplitude, phase of each carrier and offset between carriers. Although multilevel inverter offers several advantages, the control strategies of MLI are quite challenging due to the complexity to cater the transitions between the voltage levels (or steps).A number of modulation strategies are used in multilevel power conversion applications. In this proposed topology two methods are used.

a) Equal Amplitude Carriers

b) Un Equal Amplitude Carriers (or) Variable Amplitude Carriers (VAC)

EQUAL AMPLITUDE CARRIERS (EAC)

In this method, all the triangular carriers used will have the same amplitude. The PWM methods used are PDPWM, PODPWM, APODPWM, COPWM, PSPWM and VFPWM with sine, THI, trapezoidal, TAR and stepped wave references. Figures 2 to 4 shows the sample carrier arrangement, output voltage and FFT plot for PDPWM strategy with sine reference (m_a = 0.8 and m_f=20). Where m_a and $m_f$are the amplitude and frequency modulation index.

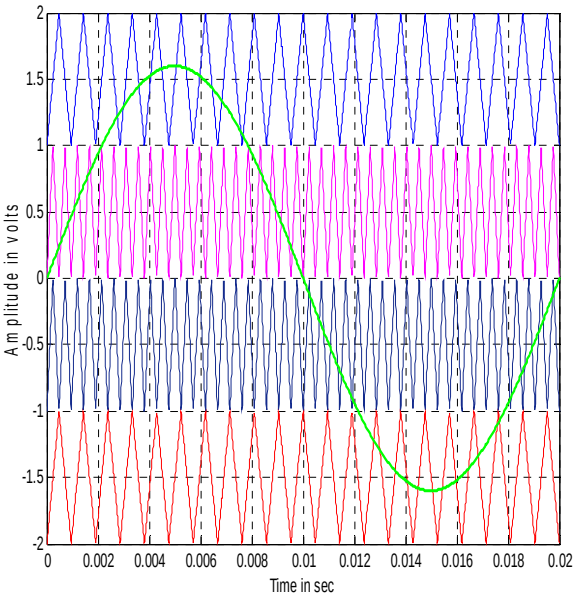

Figure-2. Sample carrier arrangement for equal amplitude carriers with VFPWM strategy (sine reference for m_a = 0.8, m_{f1} = 20 and m_{f2} = 40).

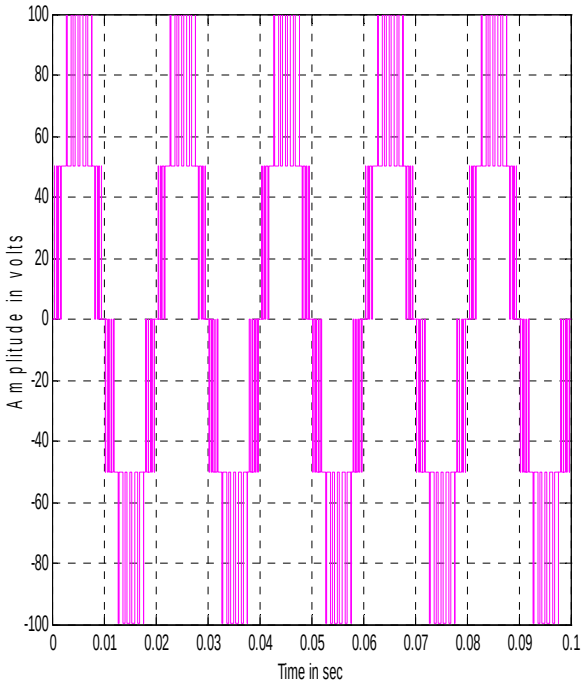

Figure-3. Sample Output voltage of five level inverter based on equal amplitude carriers with VFPWM strategy (sine reference for m_a = 0.8, m_{f1} =20 and m_{f2} = 40).

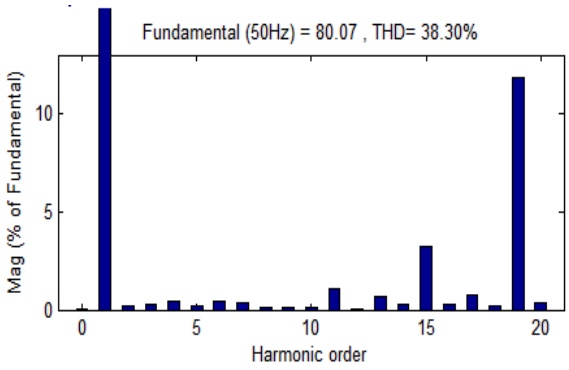

Figure-4. Sample THD plot for five level output voltage based on equal amplitude carriers with VFPWM strategy (sine reference for m_a = 0.8, m_{f1} =20 and m_{f2} = 40).

UN EQUAL AMPLITUDE CARRIERS (UEAC) (OR) VARIABLE AMPLITUDE CARRIERS (VAC)

In this method, all the triangular carriers used will not have the same amplitude. The PWM methods used are UEAPD (Un Equal Amplitude Phase Disposition) PWM, UEAPODPWM, UEAAPODPWM, UEACOPWM, UEAPSPWM and UEAVFPWM with sine, THI, trapezoidal, TAR and stepped wave references. Figures5 to 7 shows the sample carrier arrangement, output voltage and FFT plot for PDPWM strategy with sine reference

(m_a= 0.8 and m_f=20). Figures 8 to 11 shows the sample reference waveforms. The following parameters are used for the simulation V_{dc}= 200V, R (Resistance) = 100 ohms, $C_1 = C_2 = C_3 = C_4 = 1000^{e-3}$, A_c (Amplitude of the carrier signal) = 0.5, 1 and 1.5, A_m (Amplitude of the modulating signal = 2, f_c (frequency of the carrier signal) = 1000 Hz and 2000Hz and f_m (frequency of the modulating signal) = 50 Hz. m_a is varied from 1 to 0.6 for equal amplitude carrier methods. In EAC method if m_a is varied from 1 to 0.51 then the inverter will work as a five level inverter and if the m_a is varied from 0.5 to zero then the inverter will work as a three level inverter. But in case of UEAC method if m_a is varied from 1 to 0.26 then the inverter will work as a five level inverter and if the m_a is varied from 0.25 to zero then the inverter will work as a three level inverter.

Where

$$m_a = \frac{A_m}{A_c} \quad (1)$$

$$m_f = \frac{f_c}{f_m} \quad (2)$$

m_{f1} = Frequency modulation index for upper and lower carriers.

m_{f2} = Frequency modulation index for intermediate carriers.

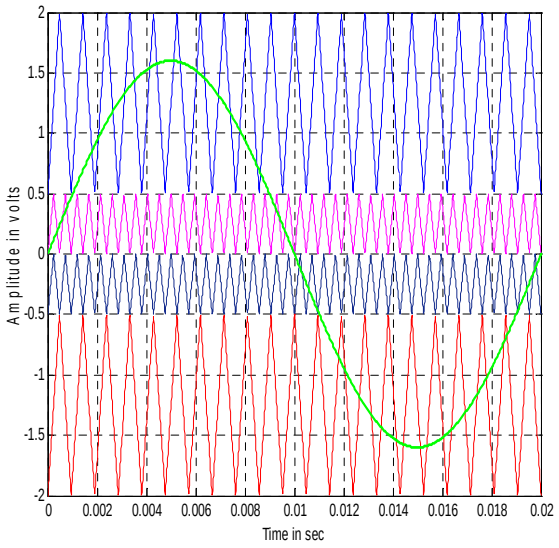

Figure-5. Sample carrier arrangement for unequal amplitude carriers with VFPWM strategy(sine reference for m_a = 0.8, m_{f1} =20and m_{f2} = 40).

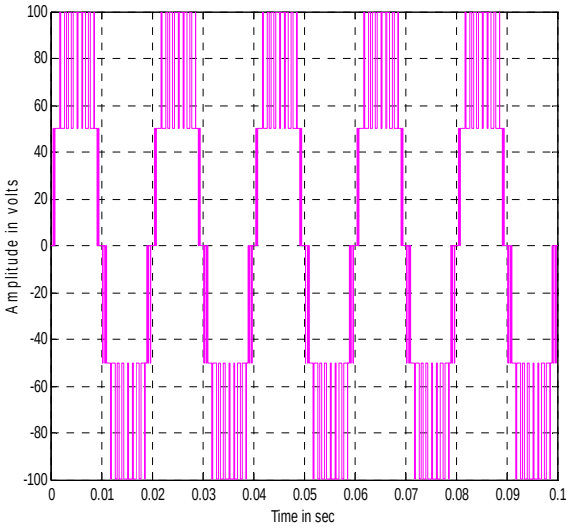

Figure-6. Sample output voltage of five level inverter based on unequal amplitude carriers with VFPWMstrategy (sine reference for m_a = 0.8, m_{f1} =20and m_{f2} = 40).

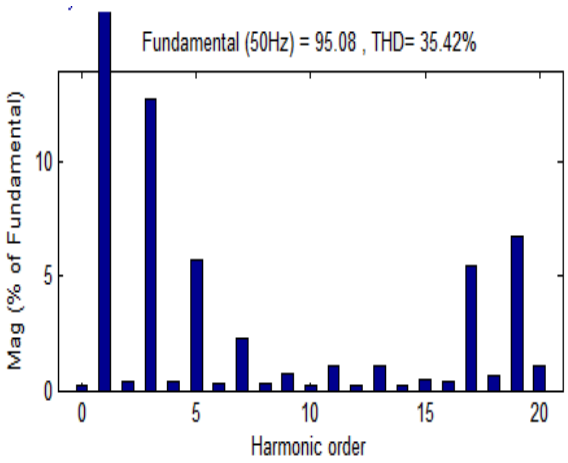

Figure-7. Sample THD plot for five level output voltage based on unequal amplitude carriers with VFPWMstrategy (sine reference for m_a = 0.8, m_{f1} =20and m_{f2} = 40).

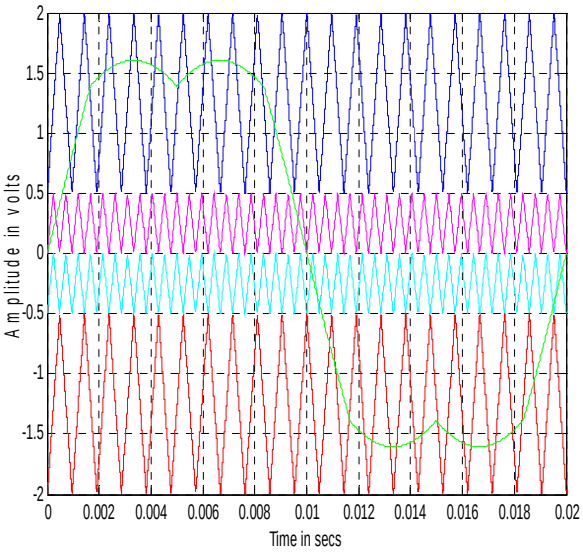

Figure-8. Sample carrier arrangement for equal amplitude carriers with VFPWM strategy (THI reference for m_a = 0.8, m_{f1} =20 and m_{f2} = 40).

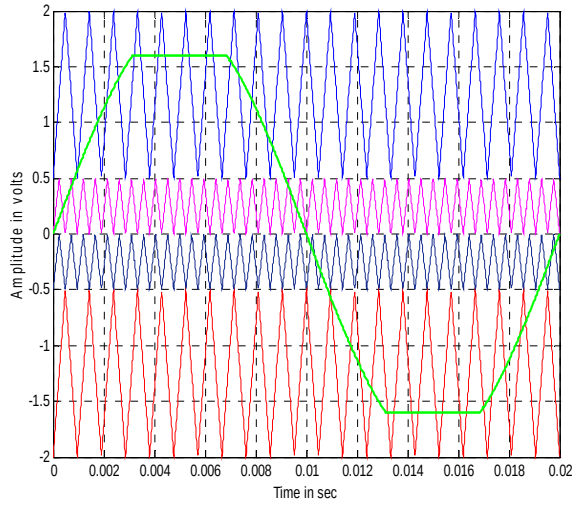

Figure-9. Sample carrier arrangement for equal amplitude carriers with VFPWM strategy (trapezoidal reference for m_a = 0.8, m_{f1} =20 and m_{f2} = 40).

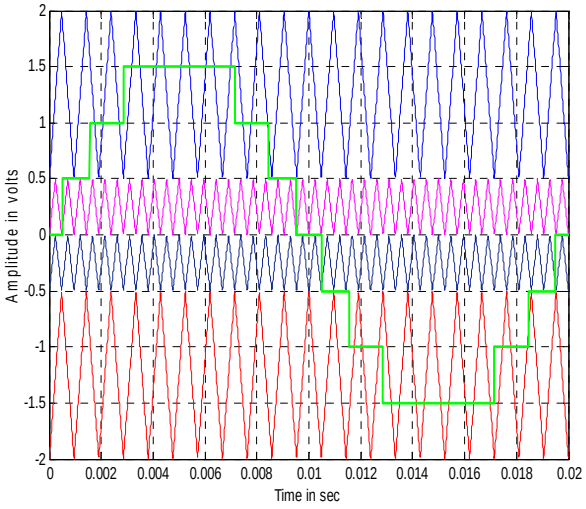

Figure-10. Sample carrier arrangement for equal amplitude carriers with VFPWM strategy (stepped wave reference for m_a = 0.8, m_{f1} =20 and m_{f2} = 40).

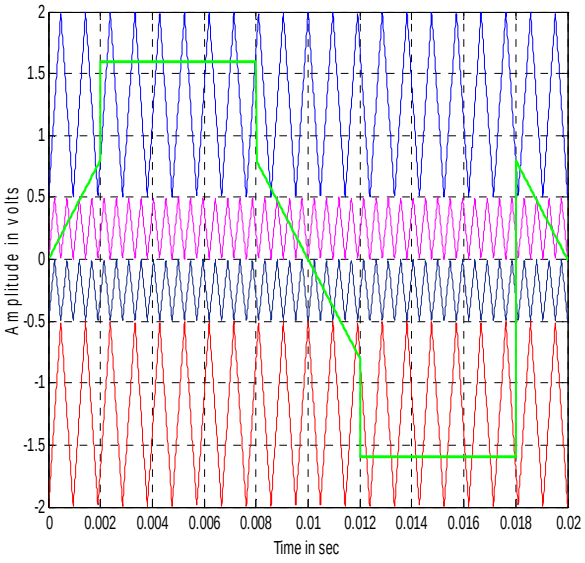

Figure-11. Sample carrier arrangement for equal amplitude carriers with VFPWM strategy (TAR reference for m_a = 0.8 , m_{f1} =20 and m_{f2} = 40).

Table-1. THD for five level output voltage based on equal amplitude and un equal amplitude carriers with various modulation indices.

Ref.	m_a	% THD for a 5-level inverter											
		PDPWM		PODPWM		APODPWM		COPWM		PSPWM		VFPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	CO	UEACO	PS	UEAPS	VF	UEAPD
Sine reference	1	26.78	29.59	26.79	27.69	26.79	29.60	33.63	30.52	31.07	30.02	26.76	28.18
	0.9	32.95	33.59	32.99	31.65	33.00	33.61	38.54	34.71	40.07	35.22	33.36	32.11
	0.8	38.25	37.13	38.26	35.10	38.26	37.15	43.88	38.10	46.23	39.58	38.30	35.42
	0.7	41.78	40.27	41.78	38.05	41.78	40.27	49.37	40.69	51.47	44.16	42.14	38.24
	0.6	44.33	42.00	44.34	39.35	44.34	42.00	58.96	43.16	52.76	47.83	44.56	39.71
	0.5	3-level	43.25	3-level	40.36	3-level	43.25	3-level	44.57	3-level	52.59	3-level	40.39
	0.4		43.34		40.30		43.34		45.62		55.67		40.41
	0.3		43.36		42.49		43.36		48.76		70.58		42.77
THI reference	1	27.45	32.15	27.76	32.28	27.76	32.28	33.28	33.54	30.64	31.98	28.19	31.30
	0.9	35.35	35.60	35.55	35.64	35.55	35.64	37.74	37.78	39.71	37.02	35.79	36.20
	0.8	41.11	39.73	41.17	39.81	41.17	39.81	41.44	41.33	47.82	42.33	41.30	40.40
	0.7	43.80	43.10	43.80	42.01	43.80	43.21	45.63	44.73	53.07	46.85	44.06	43.76
	0.6	42.58	44.98	42.59	38.87	42.59	45.14	52.47	47.13	52.59	50.19	42.81	45.64
	0.5	3-level	45.45	3-level	41.49	3-level	45.72	3-level	58.72	3-level	54.72	3-level	46.22
	0.4		44.43		68.27		44.49		48.30		55.99		44.80
	0.3		48.86		68.87		48.87		51.51		62.37		49.20
Trapezoidal reference	1	37.34	36.65	37.30	36.75	37.30	36.75	39.54	38.38	43.93	39.23	37.64	37.25
	0.9	36.67	35.48	36.63	35.63	36.63	35.63	39.41	37.46	43.13	38.54	36.80	36.12
	0.8	36.32	34.46	36.30	34.63	36.30	34.63	40.37	36.98	43.23	37.71	36.52	35.10
	0.7	37.08	34.19	37.10	34.41	37.10	34.41	42.44	37.31	44.96	38.70	37.26	34.75
	0.6	40.91	37.34	40.91	37.39	40.91	37.39	48.18	39.89	50.61	43.01	41.10	37.60
	0.5	3-level	39.35	3-level	39.35	3-level	39.35	3-level	43.40	3-level	47.83	3-level	39.71
	0.4		40.24		40.27		40.27		46.42		53.88		40.53
	0.3		40.24		40.24		40.24		51.01		56.60		40.46
Stepped wave reference	1	24.34	26.40	24.36	26.44	24.36	26.44	33.41	30.53	29.13	30.92	24.27	26.40
	0.9	31.24	30.38	31.26	30.39	31.26	30.39	39.88	34.81	37.50	34.29	31.25	30.38
	0.8	37.45	34.43	37.43	34.45	37.43	34.45	45.59	40.16	45.91	41.84	37.45	34.43
	0.7	38.51	34.83	38.51	34.85	38.51	34.85	51.71	41.71	47.83	43.74	38.46	34.83
	0.6	37.49	39.39	38.19	39.42	38.19	39.42	67.84	49.16	45.64	52.19	38.19	39.39
	0.5	3-level	36.84	3-level	36.87	3-level	36.87	3-level	49.79	3-level	53.80	3-level	36.84
	0.4		33.37		33.37		33.37		59.95		64.38		33.37
	0.3		29.05		29.05		29.05		73.45		73.75		29.05
TAR reference	1	34.86	37.40	34.85	37.70	34.93	37.08	42.01	38.88	34.54	35.84	34.87	37.28
	0.9	43.01	42.62	43.22	42.83	42.53	42.00	46.91	43.45	45.18	41.10	43.02	42.54
	0.8	49.33	46.96	49.75	47.13	48.51	46.16	51.40	47.95	54.45	46.30	49.42	46.83
	0.7	53.66	50.27	54.22	50.42	52.69	49.27	55.55	52.21	61.18	51.36	53.71	50.33
	0.6	53.96	52.64	54.66	52.44	52.57	52.20	58.79	55.80	64.45	56.71	54.14	52.67
	0.5	3-level	54.13	3-level	53.96	3-level	53.92	3-level	58.37	3-level	61.43	3-level	54.17
	0.4		54.29		54.80		53.27		60.18		67.40		54.53
	0.3		50.83		51.65		49.27		61.11		66.92		51.09

Tables 1 and 2 shows the THD and V_{RMS} values for the proposed five level inverter. In tables it is represented as 3-level for m_a = 0.5 to 0.3. The equal amplitude carrier methods will give five levels only up to

m_a = 0.59 but the UEAC method will give five levels up to m_a = 0.26. The Tables compare the total harmonic distortion and voltage in terms of RMS for various references and carriers.

Table-2. V_{RMS} fundamental for five level output voltage based on equal amplitude and UN equal amplitude carriers with various modulation indices.

Ref.	m_a	$V_{RMS\ (fundamental)}$ for a 5-level inverter											
		PDPWM		PODPWM		APODPWM		COPWM		PSPWM		VFPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	CO	UEACO	PS	UEAPS	VF	UEAPD
Sine reference	1	70.66	76.92	70.66	76.66	70.66	76.91	75.69	77.75	68.23	76.27	70.71	76.66
	0.9	63.61	72.24	63.6	71.96	63.6	72.24	70.71	73.14	59.78	71.15	63.52	71.91
	0.8	56.57	67.62	56.57	67.25	56.57	67.61	65.33	68.58	52.03	66.47	56.62	67.23
	0.7	49.42	62.68	49.42	62.16	49.42	62.68	59.86	64.25	43.38	60.26	49.33	62.25
	0.6	42.33	58.07	42.44	57.41	42.44	58.07	52.97	59.64	36.17	54.7	42.48	57.38
	0.5	3-level	53.31	3-level	52.32	3-level	53.31	3-level	55.1	3-level	46.89	3-level	52.37
	0.4		48.32		46.75		48.32		50.14		35.12		46.8
	0.3		43.12		40.13		43.12		44.18		25.76		40.17
THI reference	1	81.89	84.51	81.83	84.48	81.83	84.48	84.05	84.58	80.38	84.11	81.78	84.41
	0.9	73.79	78.86	73.75	78.86	73.75	78.86	78.8	79.41	71.16	79.22	73.75	79.01
	0.8	65.53	73.33	65.49	73.31	65.49	73.31	73.55	74.26	61.47	73.97	65.6	73.43
	0.7	57.28	67.91	57.28	48.24	57.28	67.88	68.04	69.15	52.01	68.26	57.26	67.99
	0.6	49.03	62.33	49.02	45.07	49.02	62.29	61.36	64.1	42.44	62.72	49.07	62.32
	0.5	3-level	57.02	3-level	40.91	3-level	56.97	3-level	58.71	3-level	55.3	3-level	56.91
	0.4		51.24		32.72		51.23		53.26		41.59		51.31
	0.3		45.07		45.07		45.07		46.2		29.66		45.12
Trapezoidal reference	1	66.11	73.85	66.14	73.82	66.14	73.82	73.59	74.76	62.68	73.99	66.08	73.93
	0.9	64.67	72.81	64.71	72.78	64.71	72.78	72.38	73.81	60.69	72.52	64.69	72.83
	0.8	62.43	71.3	62.46	71.26	62.46	71.26	70.35	72.28	58.5	70.82	62.44	71.24
	0.7	58.63	68.7	58.63	68.65	58.63	68.65	67.09	69.59	54.11	67.71	58.63	68.55
	0.6	50.93	63.36	50.93	63.35	50.93	63.35	61.26	64.89	45.5	61.88	50.9	63.39
	0.5	3-level	57.41	3-level	57.41	3-level	57.41	3-level	58.86	3-level	54.7	3-level	57.38
	0.4		51.12		51.11		51.11		52.78		44.23		51.13
	0.3		44.38		44.38		44.38		45.61		31.09		44.34
Stepped wave reference	1	71.58	77.43	71.58	77.42	71.58	77.42	76.06	77.75	68.56	76.09	71.59	77.43
	0.9	64.18	72.85	64.17	72.85	64.17	72.85	70.85	73.49	61	72.36	64.18	72.85
	0.8	56.08	66.87	56.12	66.87	56.12	66.87	64.8	67.64	51.25	66.86	56.08	66.87
	0.7	51.22	64.28	51.26	64.28	51.26	64.28	60.63	65.12	45.39	61.56	51.22	64.28
	0.6	39.69	55.72	39.6	55.72	39.6	55.72	49.53	56.67	32.78	53.88	39.6	55.72
	0.5	3-level	53.78	3-level	53.78	3-level	53.78	3-level	54.12	3-level	48.98	3-level	53.78
	0.4		47.85		47.85		47.85		46.8		38.48		47.85
	0.3		40.93		40.93		40.93		38.35		24.7		40.93
TAR reference	1	75.8	77.92	75.88	77.9	75.84	77.93	76.75	78.36	75.16	76.45	75.9	78.15
	0.9	68.38	72.98	68.37	72.85	68.53	72.99	71.97	73.78	66.42	71.56	68.41	73.16
	0.8	60.61	67.92	60.54	67.69	60.84	67.91	67.1	68.9	57.7	66.85	60.69	68.05
	0.7	52.89	62.66	52.78	62.39	53.13	62.68	62.06	63.76	49.01	62.13	52.94	62.64
	0.6	42.25	57.06	45.07	57.09	45.48	57.12	56.98	58.47	40.38	57.47	45.24	57.19
	0.5	3-level	51.47	3-level	51.63	3-level	51.61	3-level	53.1	3-level	52.55	3-level	51.59
	0.4		45.85		45.6		46.06		47.89		39.34		45.93
	0.3		40.61		40.39		40.8		43.06		27.5		40.6

CONCLUSIONS

The proposed work compares the various pulse width modulation techniques for the chosen single phase half bridge DCMLI. For all the PWM strategies and references proposed, the UEAC provides less THD and higher fundamental RMS (Root Mean Square) values except for m_a =1. For m_a =1 the EAC provides less THD (Total Harmonic Distortion) and higher fundamental RMS (Root Mean Square) values for all the PWM methods and references. Tables 1 and 2 displays the total harmonic distortion and output fundamental voltages for various PWM techniques and references.

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