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SIMULATION AND ANALYSIS OF CNTFET BASED INVERTER

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ABSTRACT

Carbon nanotubes due to its numerous extraordinary properties are turning out to be the forefront material for future electronics. In comparison to silicon based FETs, CNTFETs possesses higher k gate dielectric, quasi- ballistic transport at low voltage, higher transconductance, higher drive current, higher average carrier velocity, lower heat dissipation and higher switching speed. Due to all these advantages a lot of research has been done in modeling CNTFET based electronic devices. The high performance p type and n type single walled CNTFET devices are modeled using a Stanford UniversityVerilog code in Symica DE simulator. This paper demonstrated CNTFET inverter by serially connecting p type and n type single walled CNTFETs models in simulator. Finally, a comparative performance analysis of CNTFET inverters over conventional and multi gate MOSFET inverters has been addressed.

Keywords: CNTFETs, BSCMIG, MOSFETs, FinFETs, Symica DE, Inverter.

1. INTRODUCTION

The future of electronic industry will be paved with technologies that allow portability. For portable electronic devices, size and power dissipation are the two parameters of prime concern. The scaling of conventional planar CMOS is expected to become increasingly difficult. The channel length of metal oxide silicon based field effect transistors (MOSFETs) is limited to 10nm range and further reduction in channel length result into direct source to drain tunneling. Due to direct tunneling, gate leakage current and sub threshold leakage current increases, this in turn increases the idle power required by the device. To overcome these limitations, Multi-gate FETs such as FinFETs [1] have emerged as one of the most promising candidates, which can extend the CMOS scaling to sub-25nm regime. In FinFETs the conducting channel between source and drain is replaced by thin silicon (tens of nanometers wide) called fin instead of thick silicon layer in MOSFETs. The thin layer gate structure of FinFETs has shown a better electrical control over channel thus help in reducing the leakage currents and overcoming other short channel effects. For further scaling beyond 25 nm, conducting channel need to be replaced by carbon nanotube and such FETs are called carbon nanotube field effect transistors (CNTFETs). Due to the presence of CNTs in conducting channel CNTFETs became an attractive alternative to the conventional MOSFETs. In comparison to MOSFETs, CNTFETs possesses a very high k gate dielectric, quasi- ballistic transport at low voltage, higher transconductance (almost four times), higher drive current, higher average carrier velocity (almost twice), lower heat dissipation and higher on off current ratios. Apart from all these advantages, there are various challenges related to CNTFETs that need to be addressed before replacing it with practical transistors. These challenges includes variation in the quality of CNTs, effect of chirality on tube diameter, difficulty in mass production and reliability issues due to varying environmental conditions [2],[3].

This paper presents the performance analysis of simulated model of CNTFETs based inverter in Symica DE simulator. The simulations uses the Verilog –A compact model for p type and n type CNTFETs proposed by Stanford University [4],[5]. The result of simulations demonstrates the response of CNTFETs inverter to different applied inputs. This paper also gave the comparative performance analysis of CNTFET inverters over conventional MOSFET inverters and BSCMIG (Berkeley short channel multi-gate) inverters (using Verilog –A compact model given by University of California)[6].

2. CARBON NANOTUBE FIELD EFFECT TRANSISTORS

Single walled carbon nanotubes (SWCNTs) are mostly utilized to fabricate CNTFETs. SWCNTs can be metallic or semiconductor depends on its chirality. Chirality of CNTs depend on two parameters: Chiral vector C and Chiral angle θ. Chiral vector C depends on the way the graphite sheets is rolled up to form cylinder and it is represented by a pair of chiral indices (n,m) and it is given by

$$C = na_1 + ma_2 \quad (1)$$

Where n and m denote the integer of the unit vectors along the graphene structure associated with two unit vectors a_1 and a_2 respectively.

While chiral angle θ is an angle at which graphene sheet is rolled up to form a carbon nanotube and it is given by

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}m}{m+2n}\right) \quad (2)$$

On the basis of C and θ, CNTs are classified into three types: Zigzag (θ=0, m=0), Arm Chair (θ=30°, n=m) and Chiral CNTs ($0 < \theta < 30°$, $n \neq m$) [7].A SWNT behave as metal if the value of n-m is divisible 3. Otherwise it behaves as semiconductor with small band energy gap

varying from 0.1 to 2eV.Mostly all the armchair CNTs are metallic, one third zigzag and chiral CNTs are metallic while rest two third would be semiconducting with a very small band energy gap. The diameter of CNT also depends on its chirality and it is given by

$$d = \frac{\sqrt{3}a_c}{\pi}\left(\sqrt{n^2 + nm + m^2}\right) \quad (3)$$

Where d is the diameter of tube and a_c is the bond length of carbon atoms, which is nearly equal to 1.44 Å for nanotubes. For armchair tube

$$(n=m),\ d = \frac{3a_c}{\pi} n \quad (4)$$

For zigzag tube

$$(m=0),\ d = \frac{\sqrt{3}a_c}{\pi} n \quad (5)$$

In CNTFETs, pure semiconducting SWCNT of specific dimension (depends on its chirality) is used as a conducting channel between source and drain in conventional silicon MOSFET. The operation of CNTFET is similar to MOSFET whereas in place of bulky silicon channel, thin CNT film channel carry electrons from source to drain terminal. The threshold voltage of CNTFET is defined as gate to source voltage, which is required to turn on and off the transistors. CNTFETs possess a unique property according to which its threshold voltage can be controlled by changing its chiral vector and diameter. The threshold voltage of CNTFET is given by

$$V_{threshold} = \frac{a\,V_\pi}{\sqrt{3}\,e\,d} \quad (6)$$

Where V_π is the bond energy of carbon atoms, a=2.49 Å is the lattice constant and e is the electron's quantity of the electricity .The threshold voltage of CNTFETs is higher when the difference of chiral vector (m,n) is small and viceversa. In contrast to MOSFET, threshold voltage of CNTFETs increases with the decrease in diameter of tube. On reducing the channel length of CNT from 20nm to 10nm the threshold voltage of CNTFETs increases rapidly. This increase in threshold voltage result into low leakage power which enhances its device performance [8].

3. SIMULATION RESULTSAND COMPARATIVE ANALYSIS

CNTFETs can be used as inverter by connecting p type and n type CNTFETs in series as shown in Figure-1 [9].

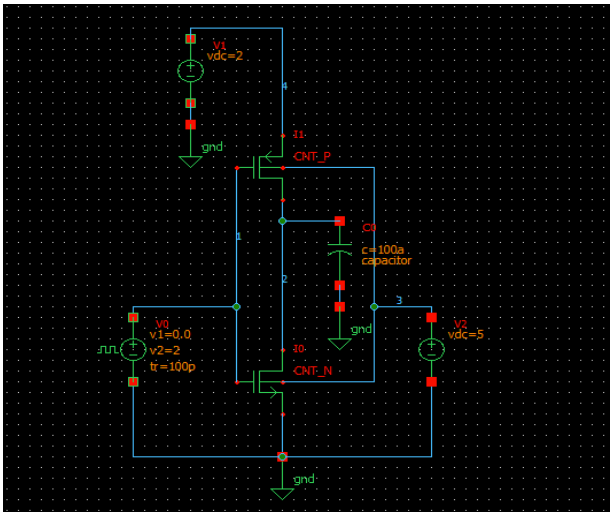

Figure-1. Schematic circuit diagram for CNTFET inverter.

The performance of CNTFET inverters, BSCMIG inverters and conventional MOSFET inverters have been analysed for three different input signals i.e. pulse, triangular and sinusoidal waveform usingSymica DE simulator. For doing these simulations, Stanford University Verilog – A compact model of CNTFETs inverter and University of California, Berkeley Verilog –A compact model of multi gate inverters have been adopted.

a) Simulated results for pulse input signal

The response of three different inverters has been analysed by applyingtrain of pulse signal of 2 V and pulse width 5nm at the input of their circuit as shown in Figure-2, 3 and 4, respectively.

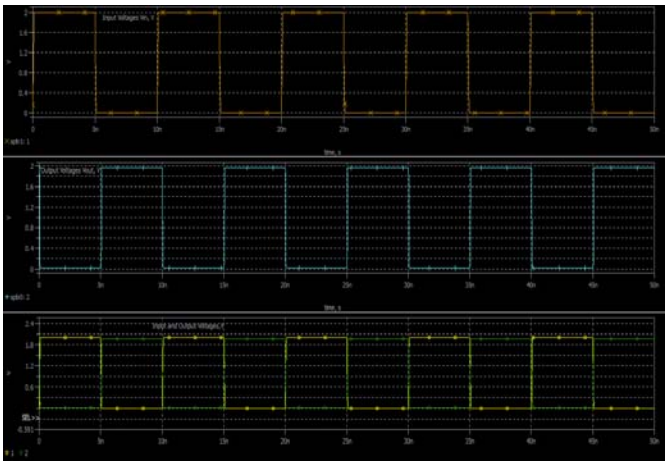

Figure-2. Simulated voltage waveforms ofCNTFETs inverter for pulse input signal.

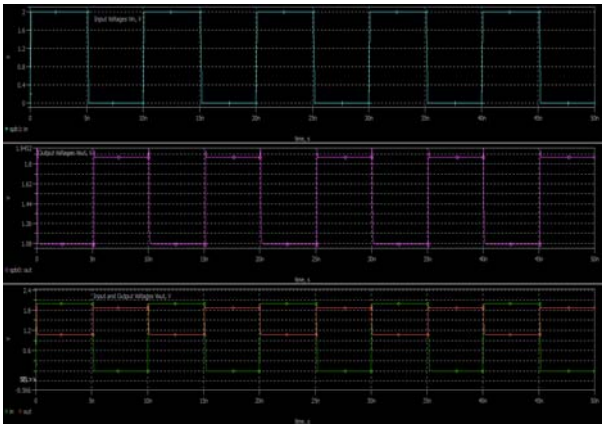

Figure-3. Simulated voltage waveforms of BSCMIG inverter for pulse input signal.

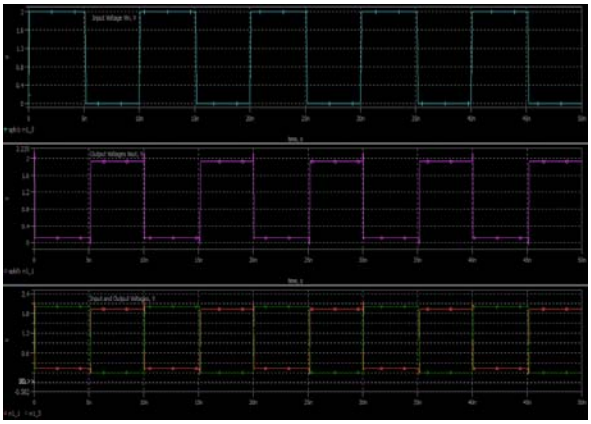

Figure-4. Simulated voltage waveforms of conventional MOSFET inverter for pulse input signal.

b) Simulated results for sinusoidal input signal

The response of three different inverters has been analysed by applying sinusoidal signal of 2 V and frequency of 10^{12} Hz at the input of their circuit as shown in Figure-5, 6 and 7, respectively.

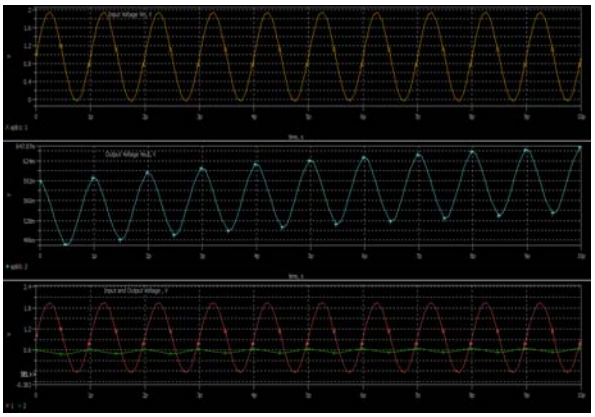

Figure-5. Simulated voltage waveforms of CNTFETs inverter for sinusoidalinput signal.

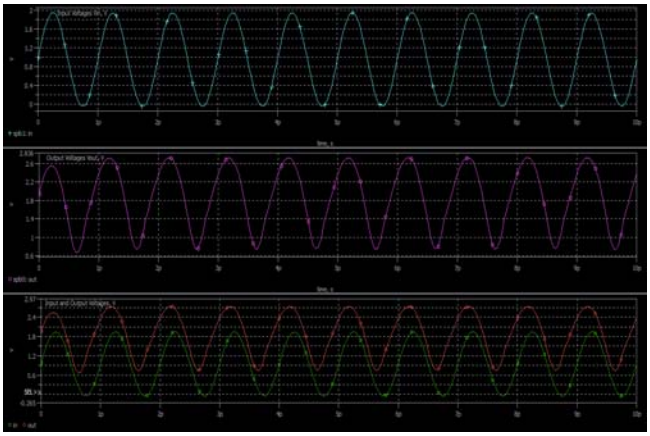

Figure-6. Simulated voltage waveforms of BSCMIG inverter for sinusoidalinput signal.

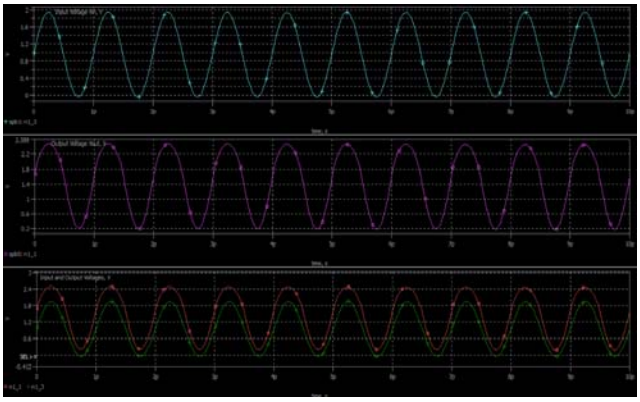

Figure-7. Simulated voltage waveforms of conventional MOSFET inverter for sinusoidal input signal.

c) Simulated results for triangular input signal

The response of three different inverters has been analysed by applying train of triangular signal of voltages V_1=0V and V_2=2V at the input of their circuit as shown in Figure-7, 8 and 9, respectively.

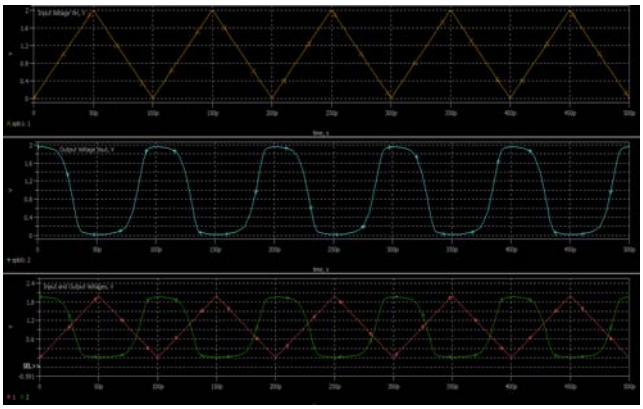

Figure-8. Simulated voltage waveforms of CNTFETs inverter for triangularinput signal.

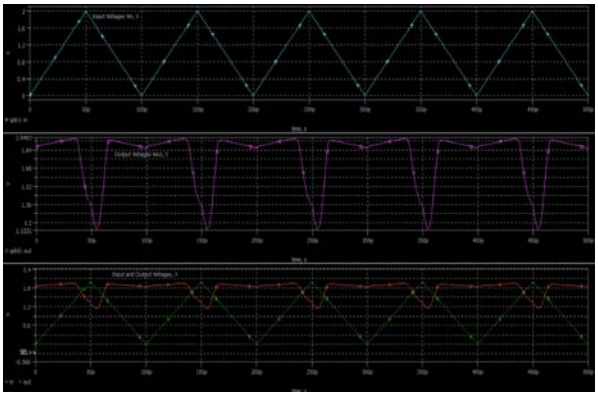

Figure-9. Simulated voltage waveforms of BSCMIG inverter for triangular input signal.

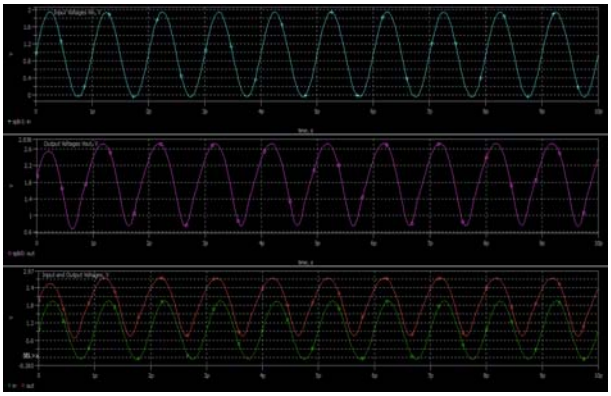

Figure-10. Simulated voltage waveforms of conventional MOSFET inverter for triangular input signal.

d. Comparative analysis

The simulated results demonstrated that out of all the three inverters, CNTFETs inverter showed best-desired response for all the three different applied inputs. And conventional MOSFET inverters have showed the worst response in all the three cases.

4. CONCLUSIONS

This paper highlighted the limitations of conventional MOSFETs at nano scales. It also discusses the basic characteristics of CNTFETs and multi gate FETs. The simulations have been performed for CNTFETs inverter, BSCMIG inverters and conventional MOSFET inverters for three different input signals using Symica DE simulator .The result of simulation confirms that at nanoscales, performance of CNTFETs inverter is better than that of BSCMIG and conventional MOSFET inverters for all the three applied inputs.

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