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SOFTWARE DEFINED RADIO IMPLEMENTATION IN 3GPP SYSTEMS

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ABSTRACT

Radio frequency can be accessed by computer through Universal Software Radio Peripheral (USRP) hardware device capability, and it is expensive for laboratory experiments, but Family Radio Service/General Mobile Radio Service (FRS/GMRS) does not use the hardware component. Software Defined Radio (SDR) provides the platform through Mat lab/Simulink tool and this is possible by the IEEEP1900.1 group. Software Defined Radio (SDR) allows different modulation technique such as Analog modulation, Quadrature phase shift keying (QPSK), Differential Binary Phase Shift Keying (DBPSK) and the Differential Quaternary Phase Shift Keying (DQPSK) implementation in the design and limitations need to overcome are hardware requirement, communications distance, static frequency offset and time-varying symbol delay through the enhancement in the receiver part. Here analog modulation (amplitude) is implemented with enhancement in the receiver part.

Keywords: radio, SDR, USRP, FRS/GMRS, DBPSK, DQPSK, QPSK, Analog Modulation.

1. INTRODUCTION

Software Defined Radio (SDR) is the radio in which some or all of the physical layer functions are Software Defined. Software Defined Radio can also be called as Software radio which refers to wireless communication in which transmitter modulation is generated (or) defined by a computer and in the receiver part it uses a computer to recover the signal intelligence. A number of definitions can be found to describe the SDR but the SDR Forum along with IEEE P1900.1 group put the definition in simple format as Radio in which some or all of the physical layer functions are software defined. It as many applications and advantages, for radio equipment manufacturers and system integrator, SDR enables the family of radio products to be implemented using a common radio source and also allows reusing the software for radio products for reducing the cost of development, for radio service providers allows new features and capabilities to be added to existing infrastructure with reduced cost and also allows the use of a common radio platform for multiple markets and for end-user it aims to enabling them to communicate whenever they need with reduced cost.

Universal Software Radio Peripheral (USRP)

It is a hardware device used to attach the radio connection to the computer for only the licensed user. This is performed using Hardware along with MATLAB/SIMULINK tool. USRP2 transmitter and receiver are released in R2011b but this also required the hardware components [1].

Family Radio Service/General Mobile Radio Service (FRS/GMRS) transmitter and receiver

Here it needs to set the channel and private codes to be matched to the receiver. In receiver the first part is Automatic Gain control used to average the magnitude samples about 1. Then in channel selectively and FM demodulation the channel is adjusted. Next, a channel selector computes the average power of the filtered signal, and if it is greater than a threshold, the channel selector determines that the received signal is from the correct channel and it allows the signal to pass through. In the case of an out-of-band signal, although the channel separation filter reduces its magnitude, it is still FM modulated and the modulating signal will be present after FM demodulation. To reject such a signal completely, the channel selector outputs zero.

The CTCSS [2] decoder computes the power at each CTCSS tone frequency using the Goertzel algorithm [3] and outputs the code with the largest power into the Decision block. The Goertzel algorithm is used because it provides an efficient method to compute the frequency components at predetermined frequencies The Decision block compares the decoded code with a preselected code and sends the signal to the audio device if the two codes match. When the preselected code is zero, it indicates no squelch system is used and the decision block passes the signal at the channel to the audio device no matter which code is used [4]. Then it is passed to the high pass filter to filter out the tones and finally it is obtained as requires signal. The main advantage of this method is that it doesn't require the hardware component to provide the radio service but the drawback is that it serves only for short distance in two-way communication and the design is complex.

The advanced version of this method is Quadrature phase shift keying (QPSK) Transmitter and Receiver is used in this paper to overcome the limitations in the existing system. It deals with wireless communication carrier frequency and phase offset; timing offset and frame synchronization [3].
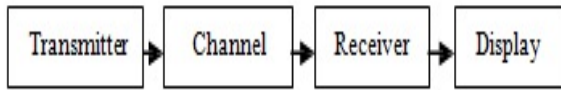
2. WORKING PRINCIPLE

Figure-1. Architecture.

The above Figure-1 represents the general architecture of SDR platform, this architecture consists of transmitter part which can be simulated in different modulation techniques and then the channel comprises of delay generator to rectify the delay between the transmitter and the channel due to the time delay [4].

The use of multiple delay characteristics allows you to investigate their effects on receiver performance, particularly on the timing recovery blocks. The delayed signal is processed through an AWGN Channel [5].
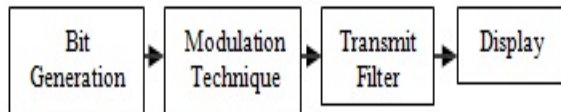
a) Transmitter

Figure-2. Transmitter.

In Figure-2 transmitter part the first block is bit generation where the Constant Barker Code is repeated twice in columns as channel (Frame based) along with output signal samples obtained from the MATLAB workspace at successive sample times and signal matrix is interpreted as one channel per column buffered into frames by specifying number of samples per frame greater than one are provided to frame conversion set to sampling mode of the output signal to sample based , then it scrambles the input data using linear feedback shift register whose configuration is specified by scramble polynomial parameter and then it is provided to the concatenate block.

In concatenate block the input signal will be of same data types to create a contiguous output signal. It may be select vector or multidimensional array mode. In vector mode, all input signal must be either vector or one-row [1*M] and one-column [M*1] or combination of vectors. The output matrix may be one-row or one-column depending upon input matrix. Then in QPSK Modulator Baseband modulates the input signal using the quaternary phase shift keying method.

Since it is the block next to the bit generation the input is binary. In raised cosine transmit filter upsampling and filtering the input signal is done using normal or square root raised cosine FIR filter. Transmitter output and spectrum scope is one form of displaying the output [6].

b) Channel

The AWGN Channel with Frequency Offset and Variable Delay subsystem first applies the frequency offset and a preset phase offset to the transmit signal as shown in the Figure-3. Then it adds a variable delay with a choice of the following two types of delay to the signal:
Ramp delay- This type of delay is initialized at Delay Start samples, and increases linearly at a rate of Delay Step samples. Triangle delay - This type of delay linearly changes back and forth between Min Delay samples and Max Delay samples at a rate of Delay Step samples.
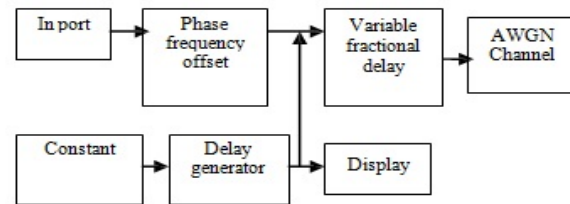

Figure-3. Channel.

The use of multiple delay characteristics allows you to investigate their effects on receiver performance, particularly on the timing recovery blocks. The delayed signal is processed through an AWGN Channel [5].

c) Receiver

The Raised Cosine Receive Filter down samples the input signal by a factor of two, with a roll off factor of 0.5 in the Figure 4. It provides matched filtering for the transmitted waveform.

The phase error detector gain of the phase and timing error detectors is proportional to the received signal amplitude and the average symbol energy. To ensure an optimum loop design, the signal amplitude at the inputs of the carrier recovery and timing recovery loops must be stable. The AGC ensures that the amplitude of the input of the Coarse Frequency Compensation subsystem is $1/Upsampling Factor$, so that the equivalent gains of the phase and timing error detectors keep constant over time. The AGC is placed before the Raised Cosine Receive Filter so that the signal amplitude can be measured with an oversampling factor of four, thus improving the accuracy of the estimate.

The Coarse Frequency Compensation subsystem corrects the input signal with a rough estimate of the frequency offset.
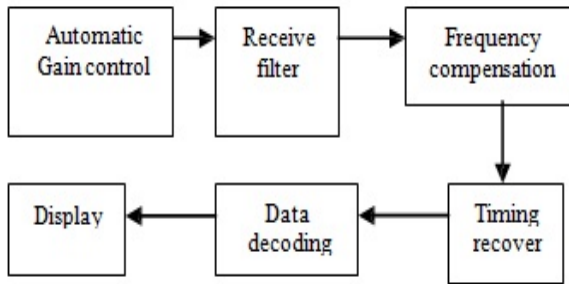
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Figure-4. Receiver.

Frequency Compensation subsystem- Subsystem uses a baseband QPSK signal with a designated phase index, frequency offset and phase offset. First, the subsystem raises the input signal to the power of four, which is not a function of the QPSK modulation. The Timing Recovery subsystem implements a PLL, to correct the timing error in the received signal. The input of the Timing Recovery subsystem is oversampled by two. On average the Timing Recovery subsystem generates one output sample for every two input samples [7].

The Data Decoding subsystem performs frame synchronization, phase ambiguity resolution, demodulation and text message decoding. The subsystem uses a QPSK- modulated Barker code, generated by the Bits Generation subsystem, to correlate against the received QPSK symbols and achieve frame synchronization [8].

3. SIMULATION ENVIRONMENT

Response for the simulation is represented in the scatter plot, display, scope and time scope.
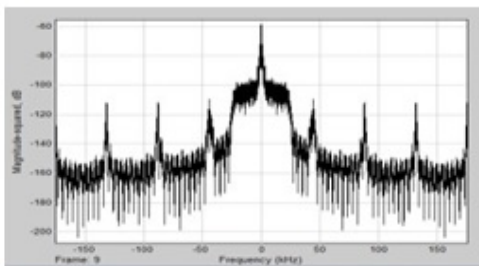
a) Spectrum scope

Figure-5. Spectrum scope after transmitter.

Spectrum scope after transmitter as shown in the Figure-5 represents the frequency usage up to 150 kHz for the frame 9.
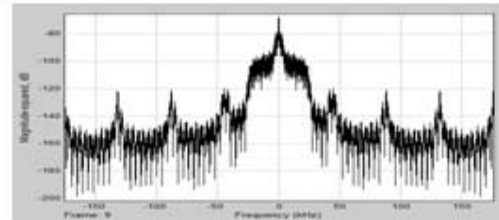

Figure-6. Spectrum scope after channel.

Spectrum scope after channel as shown in the Figure-6 represents the frequency usage up to 150 kHz for the frame 9.
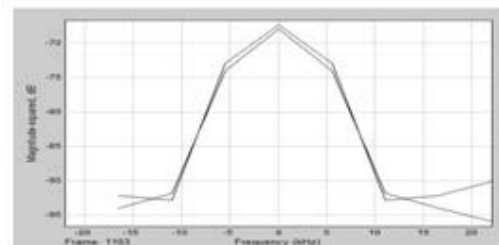

Figure-7. Spectrum scope after receiver.

Frame sequence upto 1103 the spectrum utilization is 20 kHz as shown in the Figure-7 [10].

d) Display

Display shows the value of the input with the decimation and format property. The Decimation parameter enables you to display data at every nth sample, where n is the decimation factor. The default decimation, 1, displays data at every time step. The Sample Time property enables to specify a sampling interval at which to display points. This property is useful when you are using a variable-step solver where the interval between time steps is not the same. The default sample time, -1, causes the block to ignore the sampling interval when determining the points to display.

Resizing options: If the block input is an array, you can resize the block to show more than just the first element. You can resize the block vertically or horizontally, and the block adds display fields in the appropriate direction. A black triangle indicates that the block is not displaying all input array elements. The Display block shows the first 200 elements of a vector signal and the first 20 rows and 10 columns of a matrix signal.

The Display block accepts real or complex signals of the following data types: Floating point, Built-in integer, fixed point, Boolean and Enumerated [9].
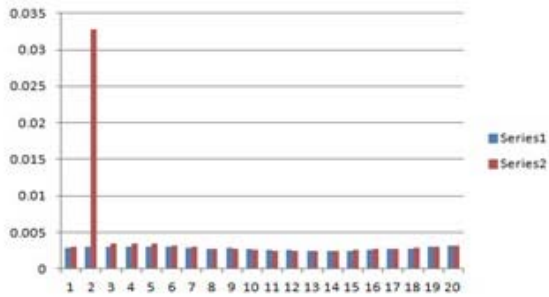
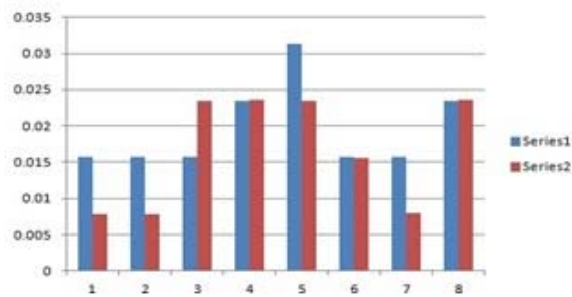**Figure-8.** Display properties for transmitter and channel.

Figure-9. Display properties for the receiver.
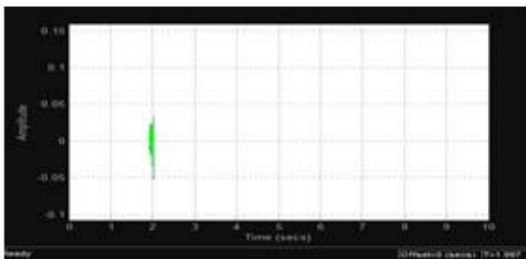
e) Time scope

Figure-10. Time scope for the transmitter.

Time scope for the transmitter in the Figure-10 represents the signal in the time domain for about 2 in the time sequence and the amplitude occupied is less than 0.05.

Simulation status: provides the current status of the model simulation. The status can be one of the following conditions:
Initializing, Ready, Running and Paused. The Simulation Status is part of the Status Bar in the Time Scope window.
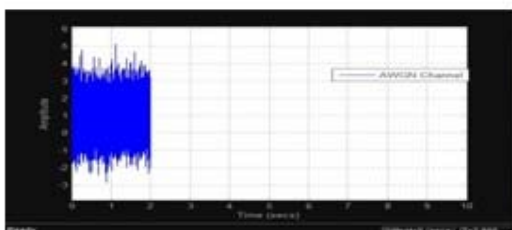

Figure-11. Time scope for the channel.

Time scope for the channel in the Figure-11 represents the signal in the time domain for about 2 in the time sequence and the amplitude occupied is 3.

Time offset: The Time offset value helps you determine the simulation times for which the scope is displaying data. The value is always in the range $0 \leq$ Time offset$\leq$ Simulation time. For example, if you set the Time span to 20 seconds, and you see a Time offset of 0 (secs) on the scope window, the scope is displaying data for the first 0 to 20 seconds of simulation time. When you see the Time offset change to 20 (secs), the scope is displaying data for simulation times is greater than 20 seconds and less than or equal to 40 seconds. The scope continues to update the Time offset value until the simulation is complete.

Simulation time: when the model is running or simulation has been paused, the scope displays the current simulation time. If the model simulation completes or is stopped, the scope displays the time at which the simulation stopped. The Simulation time is part of the Status Bar in the Time Scope window.
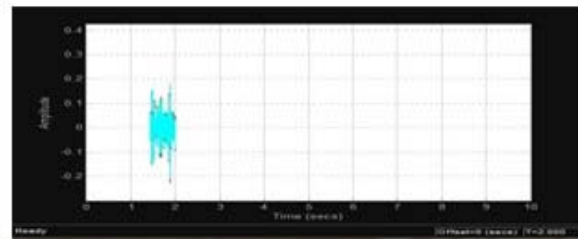

Figure-12. Time scope for the receiver.

Time scope for the receiver in the figure 12 represents the signal in the time domain for about 2 in the time sequence and the amplitude occupied is 0.2 [11].

4. CONSCLUSIONS

From the above Simulink response, physical layer transmitter parts are modeled using MATLAB and implemented in SIMULINK ENVIRONMENT. Applying the Software Defined Radio (SDR) technology in the implementation of this promising standard facilitates the anticipated modifications and enhancements to the receiver part will occur to that standard using the modulation techniques. The comparisons for the transmitter, channel and receiver are specified using the excel sheet and also viewed in display block.

5. FUTURE WORK

The enhancement can be done with the other modulation techniques in the transmitter part. The Performance can also be analyzed along with different channel blocks in the channel part along with modifications in the transmitter and receiver.

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