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MODEL-BASED DESIGN OF LTE BASEBAND PROCESSOR USING XILINX SYSTEM GENERATOR IN FPGA

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ABSTRACT

Long Term Evolution (LTE) is likewise brought up to as Evolved - Universal Terrestrial Radio Access (E-UTRA). The specifications define a new physical air interface in order to increase of the data rate of the cellular mobile wireless. In this paper, to appraise the effectiveness of LTE physical layer, the Reed-Solomon coder is used for Forward Error Correction (FEC) in systems where the data are transferred and vulnerable to errors before the reception. In an indispensable of convolution encoder, based on the encoder output rate more than to 2 bits are sent over the channel for every input bit. It is employed in a full combination of error correcting applications and frequently used in terminal with the Viterbi Decoder. These subsystems are implemented in MATLAB/Simulink model based design and the analysis of power parameter like Total power, Thermal power, Quiescent, Dynamic with family package in the Xilinx System Generator (XSG), and realize with FPGA.

Keywords: LTE, RS Outer Coder, FEC, Viterbi Decoder, XSG, FPGA.

1. INTRODUCTION

The major development in communications networks was born when the Third-Generation Partnership Project (3GPP) started its work to define a technical standard for the so-called Beyond 3G (B3G) systems [9]. The expansion of cellular services with 4G technologies like Long Term Evolution (LTE) depends on the availability of the right sort of the spectrum. The goal of LTE is to increase the capacity and speed of wireless data networks using new Digital Signal Processing (DSP) techniques and modulations that were developed in the beginning of the new millennium [6]. LTE has been developed by the 3rd Generation Partnership Project (3GPP) to offer a fully 4G-capable mobile broadband platform [10]. LTE is an Orthogonal Frequency-Division Multiplexing (OFDM) based radio access technology that supports a scalable transmission bandwidth up to 20 MHz and advanced multi-antenna transmission. [1] As a key technology in supporting high data rates in 4G systems, Multiple-Input Multiple-Output (MIMO) enables multi-stream transmission for high spectrum efficiency, improved link quality, and adaptation of radiation patterns for signal gain and interference mitigation via an adaptive beam forming using the antenna arrays. [3]

In LTE physical layer one of the blocks is Forward Error Correction (FEC), which is also called channel coding is a process of controlling errors during transmission of the data. Where the sender adds systematically generated redundant data to its messages, also known as an error-correcting code using in data communication [2]. FEC is an integral part of the initial analog-to-digital conversion in the receiver. The maximum fractions of errors or of missing bits that can be corrected are determined by the design of the FEC code.In the FEC code there are Reed Solomon Encoder and Decoder, Convolution Encoder and Viterbi Decoder. In RS Encoder the data is processed to determine, whether any errors have occurred during transmission. Once the number of errors is determined, the RS Decoder decides if they are in the range of correction. After determining this, the decoder corrects the errors in the received data [2]. Convolution encoder to Viterbi decoder is a powerful method for the forward error correction technique.

The input data stream is fed to the convolution encoder, which produces an encoded output stream according to designed encoder specification. The encoded data steam travels through the channel having the presence of noise, produces the new encoded stream with noise. This noisy data is given to the Viterbi decoder that produces the corrected data which is applied to the encoder as input [4].

2. OBJECTIVE AND MOTIVATION

Implementation of LTE physical layer base band processing blocks efficiently in FPGA, so that it can be used further for integrating together in the base band processor for communication purpose. The implemented blocks are RS encoder and decoder, convolution encoder and Viterbi decoder.

The motivation of this paper is simulating the models in the MATLAB/Simulink of ISE design flow in RTL designer, net-list designer and bit stream generator. The net-list files need to be generated by an HDL simulator through the ISE [5]. The analysis of power parameter like Total power, Thermal power, Quiescent, Dynamic with family package in the Xilinx System Generator (XSG), and realize with FPGA.

The development of mobile devices is based on the evolution of transistors according to Moore's law which results in the processor and memories have the better performance with reduced size, cost and power consumption [6].

The paper covers to explain the LTE Physical layer Baseband Processor in section 3. Simulation Environment is discussed in briefly in section 4 and provides results of the power consumption, time. The conclusion is discussed in section 5. Future Scope is discussed in Section 6.

3. LTE PHY LAYER BASEBAND PROCESSOR

Figure-1 shows the block diagram of the LTE baseband system [8]. Reed-Solomon Encoder, RS decoder, Convolution Encoder with Viterbi Decoder chosen for implementation in FPGA.

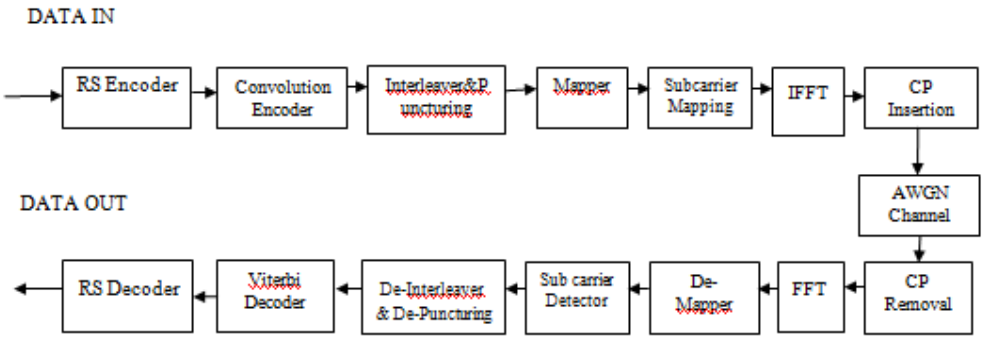

Figure-1. Block diagram of the LTE baseband system. [8]

3.1 Reed Solomon encoder

To support variable block size and therefore configurable error correction capability, puncturing and shortened codes are supported. Finally, in the IEEE802.16-2004 standard the redundant bits are sent first, while leaving the trailing byte at the end to flush the convolution encoder stage [2].

The encoder reads three message symbols, computes the parity symbols for total N symbols. Generator polynomial coefficients are given to the multiplier coefficient. The coefficients produced will be symbols such that polynomials will exactly divide the parity polynomial. The process continues till all the symbols of m(x) are given as input to the encoder. For each clock cycle parity symbol is generated. In this way we obtain the parity symbols at the last clock cycle. Hence a new block can be started at the $(n+1)^{th}$ clock pulse.

Figure-2 shows the RS encoder system. Din is the data burst after randomization. The vin to enter RS Encoder block is used for handshaking to avoid any input data being dropped when the RS Encoder is generating Parity symbols.

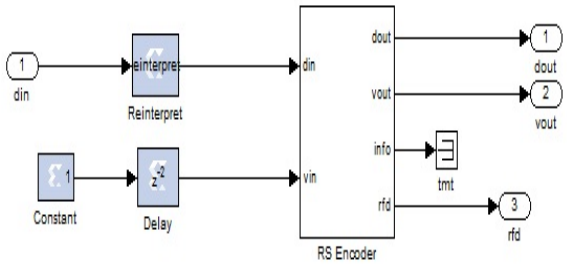

Figure-2. RS encoder system.

V out is from the rdy port of RS encoder, it marks each symbol produced on data out as valid or invalid. When vout equals 1, it means the coding is completed.

3.2 Reed Solomon decoder

The Reed-Solomon Decoder performs detection and correction of encoded data available at the receiver after demodulation. The RS encoded data is then processed to determine whether any errors have occurred during transmission. Once the number of errors is determined, the decoder decides if they are within the range of correction.

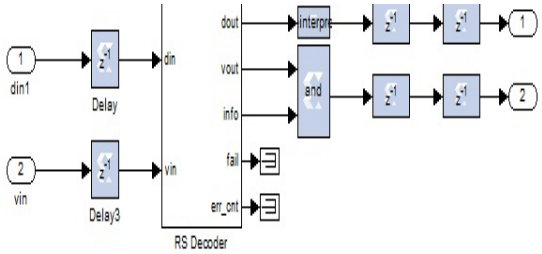

Figure-3. RS decoder system.

Before the data burst enters RS decoder, it should be processed with de-shorten. There are two steps of De-shorten shown in Figure-3. First, switch the Parity and Information Symbols. Second, append zero to let the size of data burst is 255.

Table-1. Parameters of RS encoder and decoder.

Parameters	Values
Profile (n, k, t)	(255,239,8)
Supported profile (n, k, t)	(12, 12, 0), (32, 24, 4), (40, 36, 2)

In the Table-1 are the parameters: n is a number of bytes after encoding, k is a number of data bytes before encoding, t is a number of data bytes that can be corrected where t can be expressed as t = (n-k) / 2.

3.3 Convolution encoder

With Convolutional encode data, start with k memory registers, each holding 1 input bit.[4] Unless otherwise specified, all the memory registers start with a value of 0.The Subsystem of convolution Encoder is implemented by selecting the Convolutional Encoder block produces output to the first valid data received at the input. The Delay block at the input of the encoder is used for pipelining the design. The P2S block converts the input UFIX8_0 to UFIX1_0 to serial output. In convert blocks to use rounding and saturating values require in the hardware resource shown below the Figure-4.

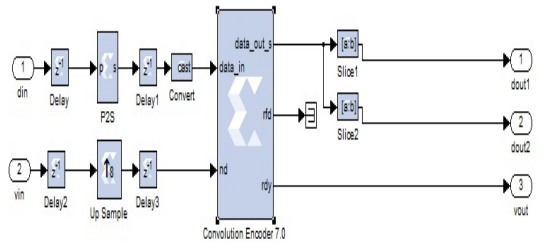

Figure-4. The subsystem of convolution encoder.

Table-2. Parameters of convolution encoder [7].

Parameters	Values
Block length	8
Code rate	1 /2
Code vectors	16
Constraint length	3

In above Table-2 are the convolution Encoder parameters after the output of RS encoding process. The input data bits are encoded by a convolution encoder that is specified where k is the convolution length of the code, then the native rate of ½ and a constraint length of 3.

3.4 Viterbi decoder

The function of Viterbi decoder is to decode the bit stream using Viterbi algorithm which has been encoded using a convolutional code. [4]

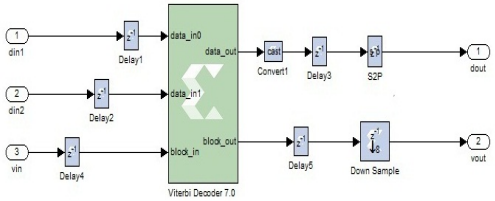

Figure-5. The subsystem of Viterbi decoder.

Figure-5 describes the Viterbi Decoder which employs soft decision decoding using the signed magnitude format for decoding. The trackback length on the Viterbi Decoder can be varied to vary the error correction capacity of the Viterbi decoder. The Viterbi Decoder block synchronizes its output to the first valid data received at the input. The Delay block at the input of the decoder is used for pipelining the design. The S2P block converts the UFIX1_0 input to UFIX8_0 for the De-Interleave block.

4. SIMULATION ENVIRONMENT

All the modules are designed in the hardware co-simulation and simulated in the Xilinx System Generator. These modules are designed in the MATLAB/Simulink and synthesized using Xilinx Integrated software environment (ISE).

4.1 Simulation results of RS encoder and decoder

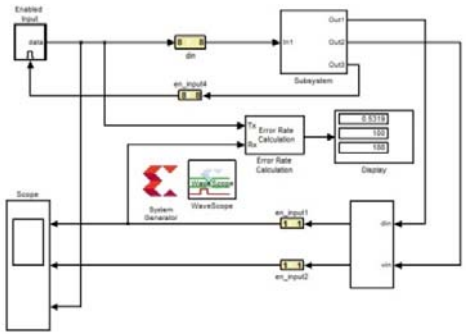

Figure-6. RS encoder and decoder with system generator.

Figure-6 shows the hardware co-simulation of RS Encoder and Decoder with continued data to the gateway which shorten the information symbols fed to the RS encoder and after decoding the same value it is De-shortened in gateway out, which is viewed in scope.

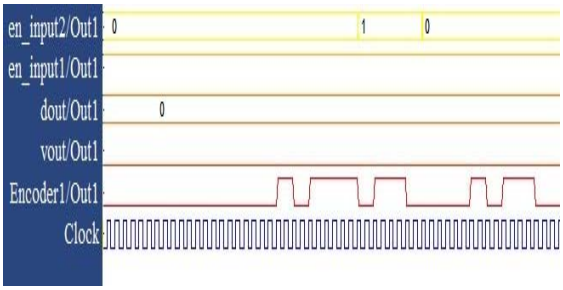

Figure-7. Waveform of RS encoder and decoder in simulink.

Figure-7 shows the Waveform of Simulink with a clock rate of 1/8 to generate the data for Error Rate Calculation.

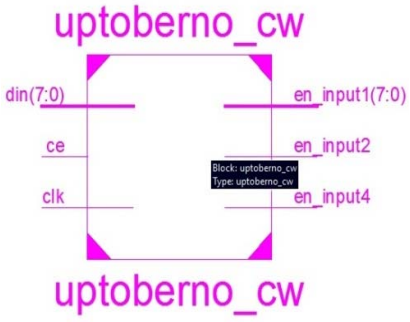

Figure-8. RTL of RS encoder and decoder.

Figure-8 shows the RTL view of RS Encoder and Decoder din input of Bernoulli binary value. Enable input is generated for every 8 clock pulses input to the block when enable is active data in.

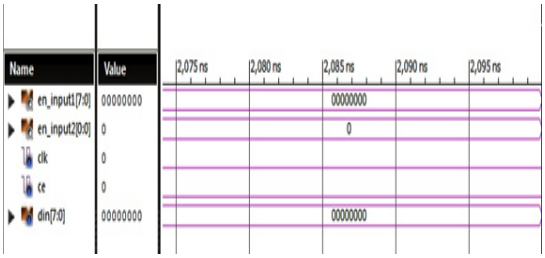

Figure-9. Waveform of RS encoder and decoder in Xilinx.

Figure-9 shows the Waveform of RS Encoder and Decoder in HDL output format using system Generator token and the syntax is checked and verify.

4.2 Simulation results of convolution encoder and viterbi decoder

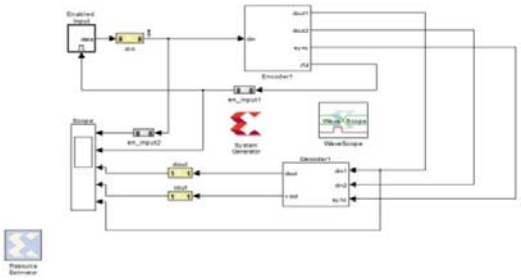

Figure-10. Convolution encoder and Viterbi decoder with system generator.

Figure-10 shows the hardware co-simulation of continuous data with gateway in which unfixed value of eight is encoded.

Figure-11. Waveform of convolution encoder and Viterbi in simulink.

Figure-11 shows the Waveform of Simulink with a clock rate of 1/8 to generate the data for Error Rate Calculation.

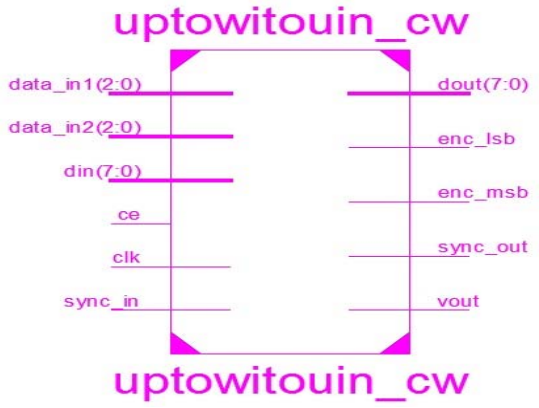

Figure-12. RTL of convolution encoder and Viterbi decoder.

Figure-12 shows the RTL view of Convolution Encoder and Viterbi Decoder. Here din input of Bernoulli binary value is Synchronized with clock and decoded.

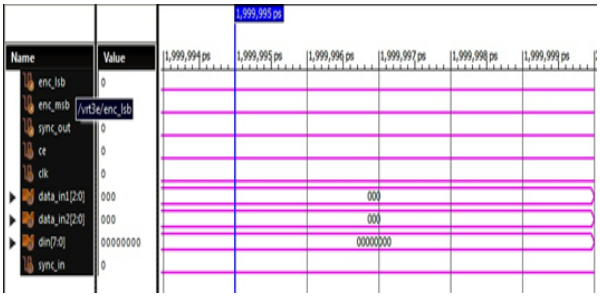

Figure-13. Waveform of convolution encoder and Viterbi decoder in Xilinx.

In Figure-13 shows the Waveform of Convolution Encoder and Viterbi Decoder in HDL output format using system Generator token and the syntax is checked and verify in the Xilinx waveform with the clock. Tables 3 and 4 analyzes in detail different level targeted device like Spartan-3E, Virtex-4, and Virtex-5. It is a comparative analysis with high performance and low power consumption in Virtex-5 with less time processing.

Table-3. Power summary.

Traget devices	Power summary							
	Rs encoder and Rs decoder				Convolution encoder and Viterbi decoder			
	Total power (W)	**Quiesent**	**Dynamic**	**Thermal power** (C)	**Total power** (W)	**Quiesent**	**Dynamic**	**Thermal power** (C)
XILINX SPARTAN 3E XC3S100e-5	0.065	0.034	0.0341	28.2	0.049	0.034	0.015	27.4
XILINX VIRTEX 4 XC4VFx100e-12	1.065	0.857	0.204	56.3	0.892	0.843	0.049	55.4
XILINX VIRTEX 5 XC5VFx100t-3	1.719	1.660	0.060	52.0	1.687	1.659	0.028	51.90

Table-4. Timing summary.

Target devices	Timing summary			
	Rs encoder and Rs decoder		Convolution encoder and Viterbi decoder	
	Minimum time (ns)	**Maximum frequency** (Mhz)	**Minimum time** (ns)	**Maximum frequency** (MHz)
XILINX SPARTAN3EXC3S100e-5	7.390	135.318	8.463	118.161
XILINX VIRTEX 4XC4VFx100e-12	5.800	181.818	5.643	177.211
XILINX VIRTEX 5XC5VFx100t-3	4.445	224.972	3.914	255.493

5. CONCLUSIONS

In the LTE Physical Layer of baseband architectures for reliable communication for which error rate calculation is essential. The blocks implemented are RS Encoder and Decoder, convolution Encoder and Viterbi decoder. To observe the errors occurring during the transmission of the data. Few addition functions should be added to the system like an interleaver and mapper. Although this architecture has limitation of increasing the number of computations by decoding the subsystem and

it provides efficient output as required power and time in SPARTAN 3E (0.049 W, 8.493 nS), and also in VIRTEX 5 (1.678 W, 3.914 nS).

5. FUTURE SCOPE

The channel estimation is also considered with higher modulation for the facility of 60MHz bandwidth in the uplink 8x4 MIMO and downlink 128-QAM. FFT and Cyclic Prefix be calculated hardware phase may be compared to the results obtained in the simulation phase, with the help of FPGA hardware.

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