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TEST VECTOR BASED MULTIPLE SOFT FAULTS DETECTION IN LINEAR ANALOG CIRCUITS WITH HARDWARE IMPLEMENTATION

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ABSTRACT

A method to detect multiple soft faults in linear analog circuits using test vectors is proposed in this paper. The circuit under test (CUT) is simulated used Modified Nodal Analysis (MNA) and with the knowledge of circuit topology and the component values, the test vectors associated with each components of the CUT and diagnosis variables are derived. In real time fault detection, the dependency of test vector to component values and tolerance limits the fault detection process in analog circuits. To solve this issue, test vectors are generated for nominal values, upper bound and lower bound values of the components of CUT and the fault detection is performed. Hardware implementation and verification of benchmark circuits such as Sallen Key Band Pass Filter and Linear Voltage Divider shows the robustness of the proposed approach in real time testing.

Keywords: analog circuits, modified nodal analysis, test vector, fault diagnosis, soft faults.

1. INTRODUCTION

Analog circuit fault detection aims to identify single or multiple, soft or hard faults of the circuit under test. Testing of analog circuits became a significant process due to non availability of standard models and procedures. Research works carried out and methodologies proposed in the field of analog circuit testing show that the factors like nonlinearity of circuit components, tolerance and the number of test nodes to locate the faulty elements, limit the development of standardized methods for testing. Faults are classified as soft faults which are due to variation in component values and hard faults which are due to open or short circuits. Different methods have been proposed to detect single and multiple soft faults in analog circuits. In [1], to improve the accuracy and efficiency of the fault diagnosis fault samples dimension is reduced by using mathematical model based on normalization algorithm. Neural network based fault diagnosis method is proposed in [2]. The structure and training methods of LVQ neural networks are presented and it has been proved to be a simple and effective practical method. In [3], Neural network based parametric fault diagnosis in analog circuit using Polynomial Curve Fitting is proposed. This method aims to cover faults as small as 10% or less. A polynomial of suitable degree is fitted to the output frequency response of an analog circuit and the coefficients of the polynomial attain different values under faulty and non faulty conditions. Using these features of polynomial coefficients, a BPNN is used to detect the parametric faults. Analog circuit fault diagnosis is also performed using evolutionary algorithms in [4]. CUT is diagnosed in the time domain. The method is based on a utilization of the tested device response and its derivative base features, i.e. following maxima and minima. The set consisted of base features are transformed into an advanced feature. Base and the advanced feature are used in fault location. The method uses fault dictionary for preliminary identification of the faults and the verification is based on the linear programming approach. Regarding to the complexity and diversity of analog circuit fault, a principal component analysis (PCA) and particle swarm optimization (PSO) support vector machine (SVM) analog circuit fault diagnosis method is proposed in [5]. It uses principal component analysis and data normalization as preprocessing, then reduced dimension fault feature is put into support vector machine to diagnosis, and particle swarm optimization is used to optimize the penalty parameters and the kernel parameters of SVM, that improve the recognition rate of the fault diagnosis. In [6], wavelet transform coefficients of the supply current and the output voltage are found. Then, distance measure is found for the faulty and fault free CUT. Then the CUT is declared as faulty if this measure for faulty CUT is greater than the measure for the fault free circuit.

In [7], multiple frequency analysis is proposed to detect single faults. The CUT is simulated using modified nodal analysis and the equations are solved using the linear system solver with Lower and Upper triangular decomposition. Testability vectors are found for all the circuit components. The tool calculates the fault variable for each test frequency and finds the average, standard deviation and coefficient of variation of the real and imaginary parts of the elements. The sum of the cumulative coefficients of variation for each element is calculated and the lowest one indicates the diagnosed faulty element. The proposed approach generates test vector as proposed as in [7], but provides solution to the challenges in real time testing.

In the following sections, detailed fault detection procedure has been explained. Section 2 describes the mathematical fundamentals of the proposed method. The challenges in real time testing, the proposed solution and test procedure adopted are explained in section 3. Section 4 explains the results obtained from hardware implementation and Section 5 deals with the discussion on the proposed approach. Section 6 concludes.

2. MATHEMATICAL FUNDAMENTALS

Analog circuit test procedure begins with the simulation of the CUT and deriving the diagnosis variables such as node voltages and branch currents. The simulation of an electronic circuit involves formulation of the circuit equation and solving it for the unknowns. To simulate the CUT, Modified Nodal Analysis (MNA) is used as explained as in [9] and [10]. MNA for linear systems results in the system equation of the form

$$AX = Z \tag{1}$$

where A is the coefficient matrix or the circuit matrix which is formed by the conductance of the components in the CUT and the interconnections of the voltage sources, X is the unknown vector consists of circuit variables (node voltages and few branch currents which are useful for testing) and Z is the excitation matrix. The right hand side matrix (Z) consists of the values of independent current and voltage sources. The unknown vector is found by matrix inverse operation. Faults in the CUT are simulated using Fault Rubber Stamp (FRS) as explained in [7-10]. FRS is based on the MNA stamp of the components of a CUT. The MNA stamp of a component C_n connected in between the nodes j and j' (V_j, V_j'- respective node voltages), in the coefficient matrix is,

$$X = \begin{bmatrix} V_n \\ I_v \end{bmatrix} \tag{3}$$

$$Z = \begin{bmatrix} I \\ V \end{bmatrix} \tag{4}$$

$$\begin{array}{c} \\ j \\ j' \end{array} \begin{array}{c} \begin{array}{cc} V_j & V_j' \end{array} \\ \begin{bmatrix} +C_n & -C_n \\ -C_n & +C_n \end{bmatrix} \end{array} \tag{5}$$

If this component is assumed to be faulty, its value changes from C_n to $C_n \pm \Delta$. This deviation causes the current through that faulty component to deviate from its nominal value. This current deviation called fault variable (ϕ) is introduced in the faulty circuit unknown matrix as an unknown branch current. To indicate the current deviation through the faulty component, the faulty component is represented as a parallel combination of its nominal value and the deviation (Δ) (Figure-1). V_j and V_j' are the node voltages at the nodes j and j' respectively. i_f is the current deviation through the faulty component.

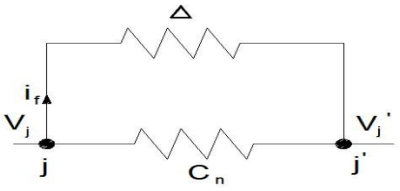

Figure-1. Faulty component representation.

The fault rubber stamp for the component C_n is,

$$\begin{array}{c} \\ j \\ j' \\ f \end{array} \begin{array}{c} \begin{array}{cccc} V_j & V_j' & & i_f \end{array} \\ \left[\begin{array}{ccc|c} +C_n & -C_n & \vdots & 1 \\ -C_n & +C_n & \vdots & -1 \\ \cdots & \cdots & \cdots & \cdots \\ \hline 1 & -1 & \vdots & -\Delta^{-1} \end{array}\right] \end{array} \tag{6}$$

The bottom row line is the faulty component equation and the right most column corresponds to the extra fault variable. As seen in (6), for each faulty component there is an additional column at the right side and row at the bottom of the coefficient matrix is introduced. The faulty system with the FRS in matrix form is,

$$\begin{bmatrix} A & c \\ r & \Delta \end{bmatrix} \begin{bmatrix} X_f \\ \phi \end{bmatrix} = \begin{bmatrix} Z \\ 0 \end{bmatrix} \tag{7}$$

where c and r are the additional column and row introduced corresponding to a faulty component. The additional column c indicates the location of the faulty component. The additional row r is the faulty component equation with its node voltages. The value of Δ depends the faulty value of the component. It can be observed that a new variable called fault variable (ϕ) is also introduced as unknown into the unknown vector matrix (X_f) of the faulty circuit. It can also be noted that this fault variable is the unknown branch current. As seen in (7), the coefficient

matrix (A) of the nominal circuit is retained in forming the faulty system equation without any modification in the values of it. Thus from (7), the faulty circuit equations are written as,

$$AX_f + c\phi = Z \quad (8)$$

$$rX_f + \Delta\phi = 0 \quad (9)$$

replacing $Z = AX$ from (1),

$$AX_f + c\phi = AX \quad (10)$$

$$A(X - X_f) = c\phi \quad (11)$$

$$X - X_f = A^{-1}c\phi \quad (12)$$

$$X - X_f = T\phi \quad (13)$$

$$\phi = (X - X_f)/T \quad (14)$$

$$T = A^{-1}c \quad (15)$$

The product $A^{-1}c$ is a complex column vector and it is called test vector [7]. As c describes the location of a component in the CUT, the test vector is associated to that component and the values are independent of the faults. Thus the fault variables which can be obtained by element wise division of the difference vector (difference between the nominal and the faulty solutions) and test vector and it leads to same column value for faulty elements as shown in Figure-3. And it can also be observed that the test vectors are associated to a specific component in the CUT and also the diagnosis variables.

3. TEST PROCEDURE

The fault variable obtained from equation (14) leads to same column value for faulty elements while testing. This is shown in Figure-3 for Sallen key Band Pass Filter (BPF). Three diagnosis variables (output node voltage, current and input node currents) are used to detect faulty components. Six components with the values R_1 = 10010Ω, R_2 = 2023Ω, R_3 = 9935Ω, R_b =10289 Ω, C_1 = 218nF, C_2 = 220nF are injected as faulty into the circuit under test. The diagnosis variables are found to have same values. But from equation (15), it can be observed that the test vector is sensitive to circuit component values (A is the circuit component matrix). In real time the nominal circuit component value itself is different from simulation because of tolerance and one may not know what exactly the component value is even for fault free circuit. Therefore when testing is performed in real time with the simulated test vectors, one cannot achieve the same results (same column value for faulty elements as in Figure-3) obtained from simulation. To solve this issue, assuming that the circuit topology and knowledge on the component tolerances is known, the test vectors are generated for nominal values, upper bound and lower bound values of the components of the CUT and real time testing is performed with these test vectors. Another problem in fault detection procedure is that the ambiguity sets. Two or more circuit components belong to same ambiguity set if a fault cannot be resolved between them. Ambiguity sets can be located with test vectors. Two elements belong to same ambiguity group if and only if their test vectors are equal [7]. This leads to the requirement of careful selection of diagnosis variables, test vectors and also more than one diagnosis variables for all component coverage.

Test procedure consists of two phases. In the pre-testing stage the circuit under test (Sallen key BPF and Linear Voltage Divider -Figure-2 andFigure-4) is simulated with its nominal values, upper bound and lower bound values and the diagnosis variables are found for fault free condition and recorded. The diagnosis variables are output node voltage (V_o), output node current (I_o), Input node current (I_i) for Sallen Key BPF and node 2 voltage (V_2) and the output voltage (V_o). These variables are chosen based on the test vector values and assuming that the nodes are accessible. The test vectors are generated using (15) for the nominal values (Tn), upper values (Tu) and lower bound values (Tl) of the components of CUT (Figures 5-9) and recorded. Figures 10 and 11 shows the test flow.In the testing stage, multiple faults with different strength is introduced into the CUT and the diagnosis variables corresponding to that fault case are measured (X_f). The fault variable matrix associated to the specified fault condition is obtained by (14) with nominal, upper bound and lower bound test vectors. The mean value of each column associated to the circuit components are obtained. The absolute mean deviation from the grand mean (population mean- mean of entire matrix) of each column is obtained and found that the absolute mean deviation is same or approximately same for faulty elements. Table-1 andTable-2 shows the results for different faulty conditions.

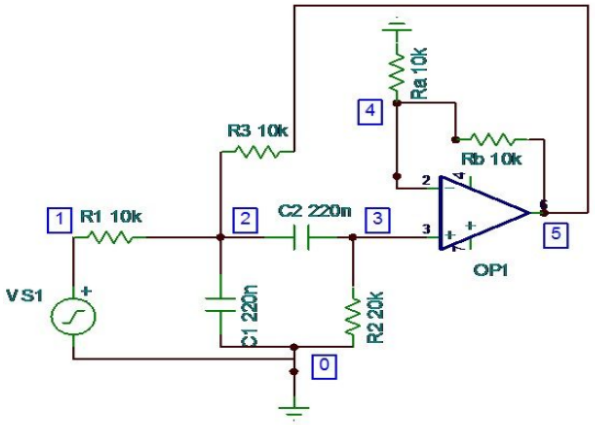

Figure-2. Sallenkey band pass filter.

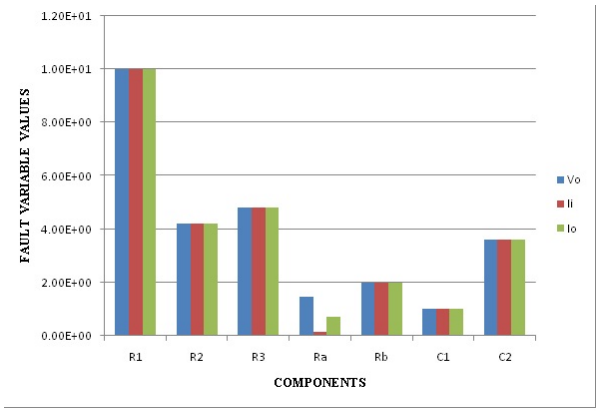

Figure-3. Six fault case-Sallenkey BPF.

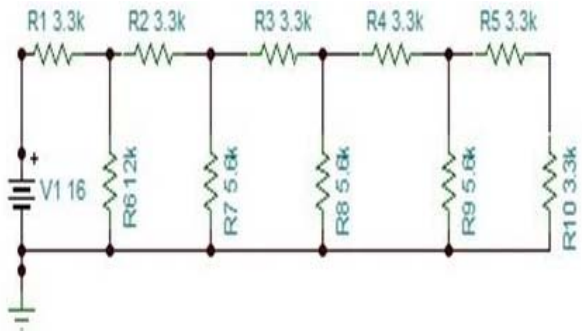

Figure-4. Linear voltage divider (LVD).

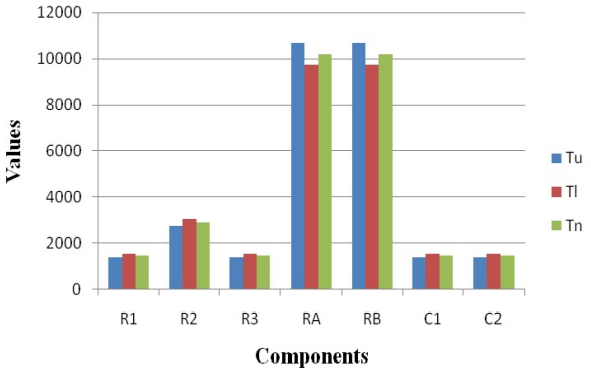

Figure-5. Test vectors of Sallen key BPF(V_5).

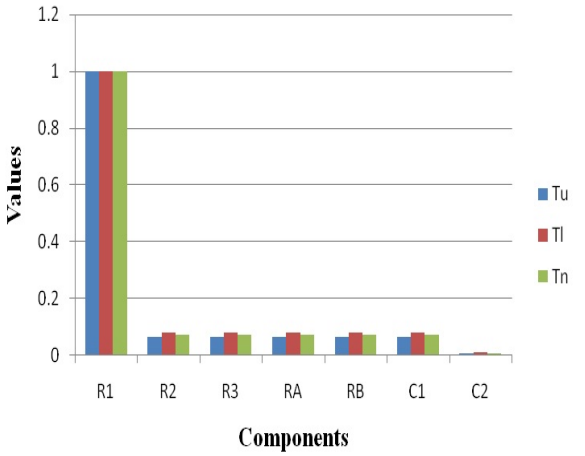

Figure-6. Test vectors of Sallen key BPF(Ii).

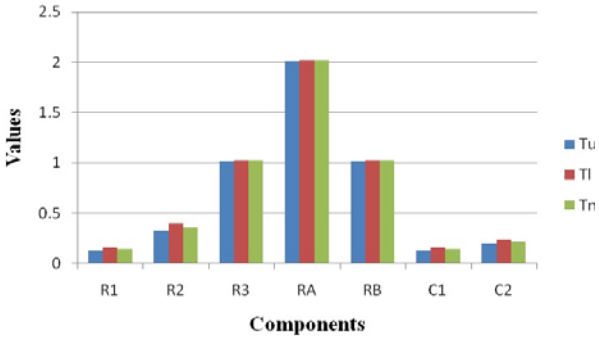

Figure-7. Test vectors of Sallen key BPF(Io).

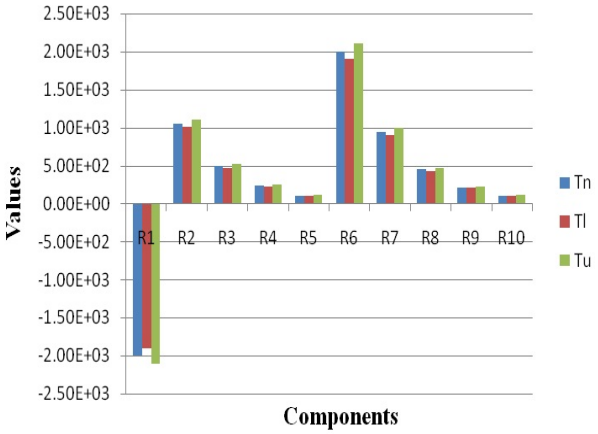

Figure-8. Test vectors (V_6) (LVD).

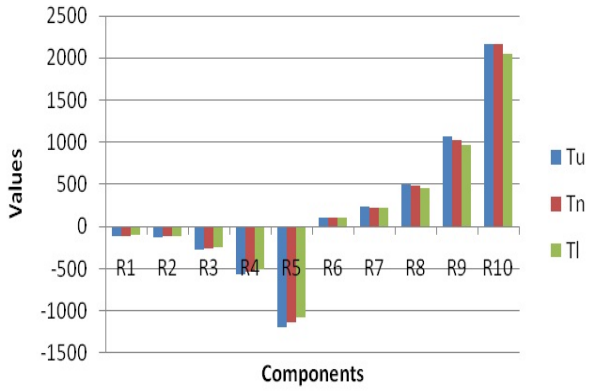

Figure-9. Test vectors (V_2)(LVD).

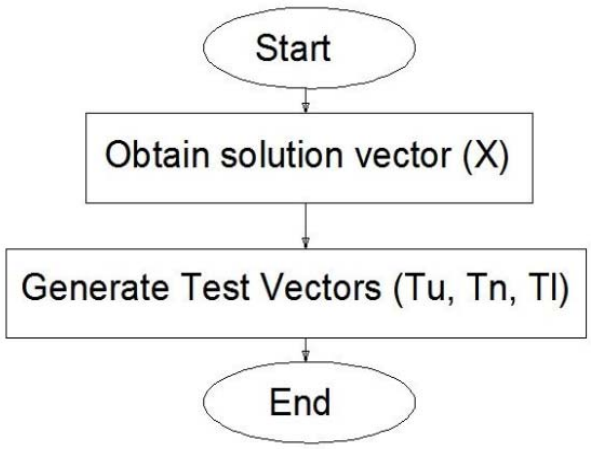

Figure-10. Pre-testing stage.

4.HARDWARE IMPLEMENTATION

4.1 Sallen key band pass filter

Figure-12 shows the hardware implementation of the CUT. A BJT based operational amplifier with input resistance 2MΩ, output resistance 75Ω and a open loop gain of 200,000 is used for testing and the circuit components with the nominal values (resistors with 5% tolerance, capacitors with 1% tolerance) as shown in Figure-2 are used and that the values (practical) are R_1 = 10.49kΩ, R_2 = 21.3kΩ, R_3= 10.1 kΩ, R_a = 9.8kΩ, R_b = 9.9 kΩ. C_1=220nF, C_2 = 220nF. Testing is performed at 1 KHz with the signal strength 10V. The diagnosis variables for the nominal, lower and upper bound values of the components are obtained from simulation are $V_{o,N}$ = 1.45, $V_{o,L}$ = 1.54, $V_{o,U}$ = 1.36, $Ii_{,N}$ = -1mA, $Ii_{,L}$ = -1.05mA, $Ii_{,U}$ = -952.38μA, $I_{o,N}$ = 72.2μA, $I_{o,L}$ =80.79 μA , $I_{o,U}$ = 64.85 μA. A CUT is said to be faulty if any one of the diagnosis variables is not inside the bound values. The diagnosis variables are measured from the hardware implementation (V_o =1.38, Ii = -953μA, I_o= 70 μA) and found to be with in the limits of fault free condition. Multiple faults with different component values are introduced in the CUT and the dianosis variables are measured and the testing procedure is followed as in Figure-11 to find the faulty component. Table-1 shows the results obtained for different faulty conditions and the absolute mean deviation is shown only for faulty component. For the faulty condition R_1 (13kΩ), R_2(10kΩ) the mean deviation is found for all the coulmn (1-7) in the fault variable matrix as (after scaling by 10^{-3}) 2.16, 1.98, 1.1, 3.2, 0.1, 0.01, 7.3, 11.7. From this it can be observed that the absolute mean deviation is approximately same for $R_1$and R_2.

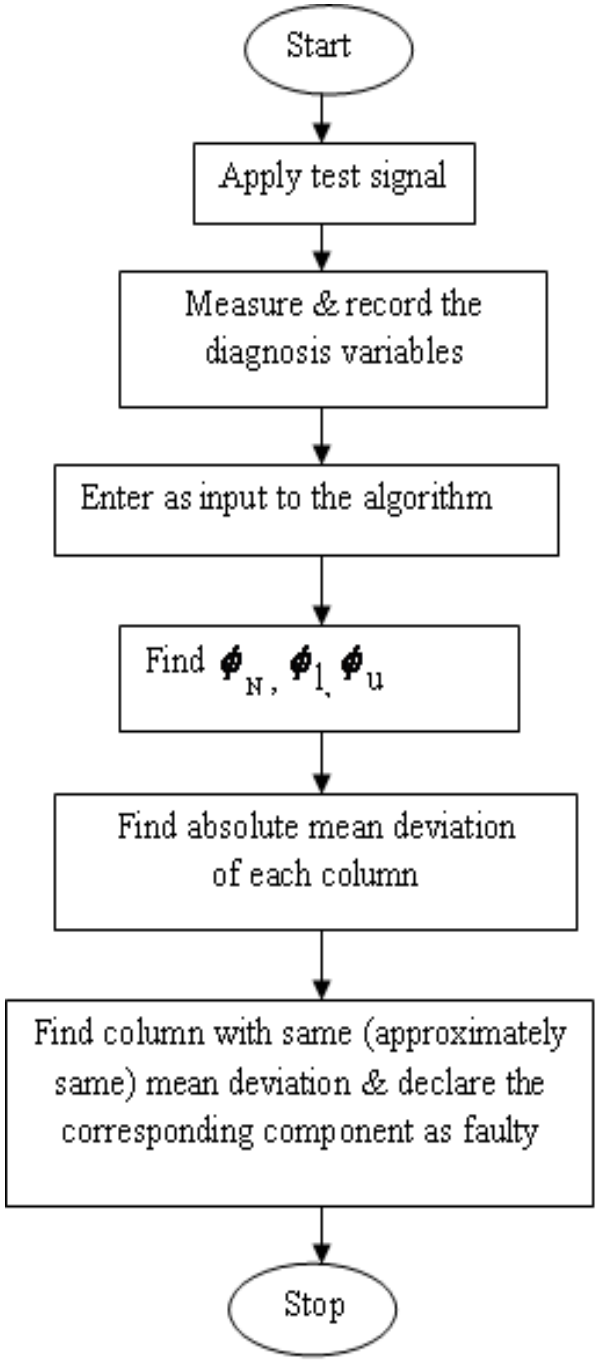

Figure-11. Testing stage.

Figure-12. Hardware implemenataion of Sallen key BPF.

4.2 Linear voltage divider

Figure-13 shows the hardware implementation of Linear Voltage Divider. The components with the nominal values are selected as in Figure-4 with the tolerance 5%. But the component values (practical) are found to be R_1=3.8 kΩ, R_2 = 3.26 kΩ, R_3 = 3.4 kΩ, R_4= 3.27 kΩ, R_5=3.19 kΩ, R_6=11.95 kΩ, R_7= 5.5 kΩ, R_8=5.47 kΩ, R_9=5.7 kΩ, R_{10}=3.29 kΩ. The diagnosis variables are measured (V_2 = 8.28V, V_o=0.443V) and they are found to be in the bound values. The diagnosis variables obtained from simulation for nominal values, upper bound and lower bound values of the components are $Ii_{,N}$ = -2mA, $Ii_{,L}$ = -1.996mA, $Ii_{,U}$ =-1.902mA, $V_{2,N}$ = 8.21V, $V_{2,L}$ = 8.21V, $V_{2,U}$ = 8.87V, $V_{o,N}$ = 0.44V, $V_{6,L}$ = 0.44V, $V_{6,U}$ = 0.44V. Multiple faults with different component values are introduced in the CUT and the dianosis variables are measured and the testing procedure is followed to find the faulty component value as in Figure-12. Table-2 shows the results obtained for different faulty conditions and absolute mean deviation is shown only for faulty components. For the faulty condition R_2 (6.5kΩ) and R_4 (3.8kΩ), the absolute mean deviation is found for all the coulmn (1 - 10) in the fault variable matrix as (after scaling by 10^{-3}) 0.9, 0.39, 2.01, 0.41, 3.2, 1.4, 4, 4.9, 0.01, 0.1.. From this it can be observed that the absolute mean deviation is approximately same for faulty components.

Figure-13. Hardware implementation of LVD.

Table-1. Results for Sallen key BPF.

Faulty component and value	Magnit ude of diagnosis variables	**Absolute mean deviation** (for faulty component) (scaled by 10^{-3})
R_1 (16k Ω), C_1 (200nF)	V_o=0.99V, I_0=51μA, I_i = -625μA	0.2, 0.18
R_3(20kΩ), C_2 (300nF)	V_o=1.4V, I_0=70μA, I_i = -951μA	1.01,0.99
R_1 (13kΩ), R_2 (10kΩ)	V_o=1.1V, I_0=56μA, I_i = -768μA	2.16, 1.98
R_a(12k Ω), C_2 (180nF)	V_o=1.3V, I_0=57μA, I_i = -950μA	0.2, 0.19
R_3 (16k Ω), C_1 (180nF)	V_o=1.7V, I_0=86μA, I_i = -950μA	0.23, 0.20
R_1 (17k Ω), C_1(240nF)C_2(190nF)	V_o=0.7V, I_0=40μA, I_i = -589μA	3.8, 3.5, 3.7
R_3 (5k Ω), C_1(280nF)C_2(190nF)	V_o=1.09V, I_0=55μA, I_i = -956μA	0.2, 0.2, 0.19
R_a(12k Ω), C_1(230nF)C_2(210nF)	V_o=1.2V, I_0=55μA, I_i = -952μA	0.2, 0.2,0.21
R_1 (8k Ω), R_3 (4k Ω)R_b(2k Ω)	V_o=1.08V, I_0=92μA, I_i = -1.25mA	2.2, 1.9, 1.8
R_2 (5kΩ), R_a(15k Ω)C_1(235nF)	V_o=1.04V, I_0=42μA, I_i = -946 μA	0.2, 0.2, 0.26

Table-2. Results for linear voltage divider.

Faulty component and value	Magnitude of diagnosis variables	**Absolute mean deviation** (for faulty component) (scaled by 10^{-3})
R_2 (6.5k Ω), R_4 (3.8kΩ)	V_2 = 9.3V, V_o=0.31V	0.39, 0.41
R_5 (1.3kΩ), R_{10} (1kΩ)	V_2 = 8.24V, V_o=0.24V	0.89, 0.9
R_7 (7kΩ), R_2 (300Ω)	V_2 = 6.77V, V_o=0.67V	1.99, 2.01
R_6 (5kΩ), R_8 (15kΩ)	V_2 = 6.82V, V_o=0.45V	2.4, 2.1
R_9 (10kΩ), R_{10} (1kΩ)	V_2 = 8.28V, V_o=0.2V	0.38, 0.401
R_8 (10kΩ), R_6 (5kΩ)R_4 (5.5kΩ)	V_2 =6.82V, V_o=0.4V	0.99, 1.1, 0.98
R_1 (500Ω), R_9 (9.5kΩ)R_5 (7kΩ)	V_2 = 14.2V, V_o=0.6V	11.7, 11.6, 11.2
R_9 (6.92kΩ), R_{10} (4kΩ)R_5 (3Ω)	V_2 = 8.28V, V_o= 0.7V	0.7, 0.69, 0.65
R_2 (9.5kΩ), R_4 (2kΩ)R_6 (3kΩ)	V_2 =6.21V, V_o= 0.19V	3.7,3.5,3.8
R_5 (8kΩ), R_7 (9.3kΩ)R_8 (1.7kΩ)	V_2 = 8.4V, V_o=0.18V	0.41, 0.40,0.38

5. DISCUSSIONS

A test approach to detect multiple faults in real time is proposed. The approach uses MNA to simulate the CUT to obtain the test vectors. Faults with different magnitude are introduced into the CUT. The diagnosis variables are recorded and the absolute mean deviation is estimated and found to be same or approximately same for faulty components. The results show effectiveness of the proposed approach in real time testing. But the approach requires more off line calculation and also careful selection of test vectors for all component fault coverage. And also the approach requires more diagnosis variables for efficient fault identification as well as all component coverage. As the fault size increases, more number of diagnosis variables with larger variation is required to effectively identify the faults because of more similar absolute mean deviation values in the columns.

6. CONCLUSIONS

A method for locating multiple faults in real time testing of analog circuits is proposed. The tolerance effect in real time testing, with the simulated test vector affects the practical possibility of implementation of test vector based testing. As explained this problem can be solved by generating the test vector for upper bound, lower bound and nominal values of the CUT. The diagnosis variables are selected based on the test vector values to solve ambiguity problems. Hardware implementation of the bench mark circuits and the results obtained shows the effectiveness of the approach.

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