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ANALYSIS OF PULSEWIDTH MODULATION CONTROL AND DIGITAL CONTROL APPROACH FOR ASYMMETRIC DC-AC CASCADED H-BRIDGE MULTILEVEL INVERTER

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ABSTRACT

This paper analyze an effective comparison between Pulse width modulation (PWM) control approach and digital control approach for asymmetric DC-AC cascaded H-bridge multilevel inverter.The conventional available approach produces 2n+1 output level for n independent DC sources and the digital control approach produces 2^{n+1}-1 output level for the same n independent DC sources with the same number switches. The proposed method also brings out the salient features of using Digital control over the conventional PWM control by producing a low total harmonic distortion level (THD) level while considering R-load. The simulation is done with the help of MATLAB and subsequently verified experimentally.

Keywords: cascaded H-bridge inverter, multilevel inverter, THD, PWM control strategy, digital control strategy.

1. INTRODUCTION

Recently, India has been put into the list of power starved country with states famished for power, also produces power cuts for about 8-10 hrs. A day, protest against the commissioning of nuclear power etc. but the need for power just grows daily which is in the range of megawatt. Considering these scenario multilevel inverters stands firmly and promises a better solution in the future. Multilevel inverters can be implemented in three different types of strategies they are diode clamped multilevel inverter, flying capacitor and cascaded H-bridge inverter. Cascaded multilevel inverter uses DC sources which are suitable for renewable energy sources such as fuel cell, hydrogen cell, photovoltaic cell and biomass. Cascaded inverters are advantages of having least number of components to achieve the required level. The soft-switching techniques can be used to reduce switching losses and the stresses in devices.

This paper analyzes and provides comparative results between the conventional PWM control and digital control approach. The conventional method available produces 2n+1 output level for n DC input but the digital technique produces 2^{n+1}-1 output level for n DC input sources.

2. MATERIALS AND METHODS

2.1 cascaded multilevel inverter

Cascaded multilevel inverter consists of n independent DC sources with n H-Bridge circuits. H-bridge consists of four switches, {MOSFET [1], IGBT, Thyristor and etc] in which two switches works in positive cycle and two switches operates during the negative cycle. Each H-bridge produces three voltage level they are $+V_{dc}$, 0,-V_{dc}.the voltage levels are produced with the different switching combination of switches in the H-bridge. Cascaded multilevel inverters can be used both in single and three phases by just adding the number of H-bridge used. The input DC source may be any DC sources such as photovoltaic cell and the final total output is the summation of individual H-bridge used .the control techniques for the H-bridge inverters are PWM technique, SVM technique etc.

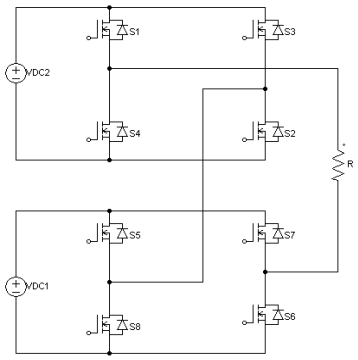

Figure-1. Cascaded multilevel inverter.

2.2. Cascaded PWM multilevel inverter

Cascaded H bridge multilevel inverter [2] comprises of a series of H bridge inverter. Cascaded inverter uses separate dc sources which can be obtained from fuel cell, hydrogen cell, photovoltaic cell etc. the cells are connected in series manner so that they add up the voltage. The main advantage of Cascaded inverter that it does not requires any voltage-clamping diodes or voltage-balancing capacitors. Considering, if there are any n level

inverters and the output voltage V_{an}= $V_{a1}+V_{a2}+V_{a3}+\ldots\ldots V_{an}$. The output of the inverter are three stages they are $+V_{dc}$, 0, and-V_{dc}. In this proposed system two H-bridge inverters were used , with each inverters has four switches, put together the circuit has eight switches they are S1,S2,S3,S4,S5,S6,S7,S8.and the two dc voltage source used are V_{dc1},V_{dc2}. The circuit diagram is shown in Figure-2and Figure-3.

The Figure-2shows the PWM multilevel inverter with R Load. Figure-3 shows the PWM control H-bridge inverter with motor as load. The conventional switching approach produces 2n+1 output for n dc sources. The proposed circuit uses 2 H-bridge inverters so for conventional PWM method the output is $2^{(2)}$+1=5output levels and the Conduction table for cascaded PWM multilevel inverter is shown in Table-1.

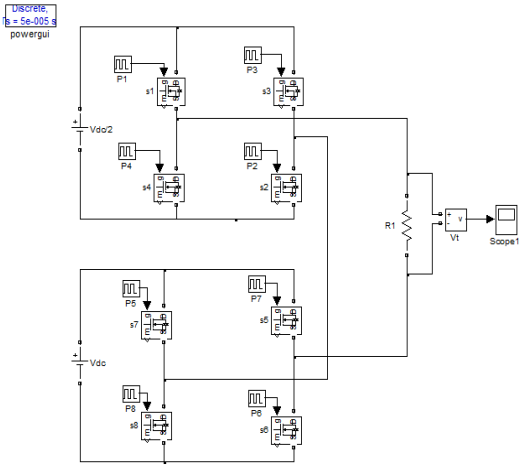

Figure-2.PWM multilevel inverter with R load.

Table-1. Conduction table for cascaded PWM multilevel inverter.

Switch/ volts	S1	S2	S3	S4	S5	S6	S7	S8
30V	1	1	0	0	1	1	0	0
20V	0	0	0	0	1	1	0	0
10V	1	1	0	0	0	0	0	0
0V	0	0	0	0	0	0	0	0
-10V	0	0	1	1	0	0	0	0
-20V	0	0	0	0	0	0	1	1
-30V	0	0	1	1	0	0	1	1

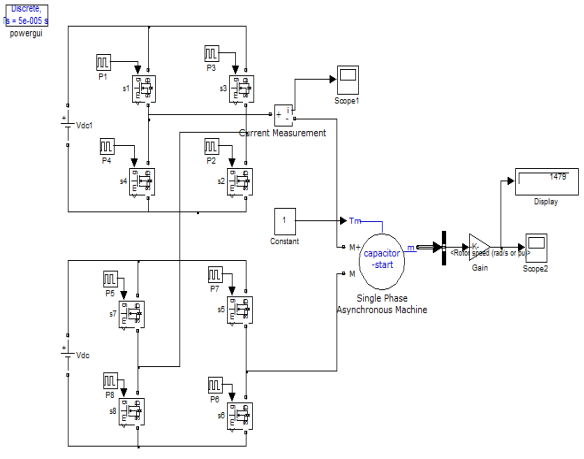

Figure-3.PWM multilevel inverter with motor load.

The Figure-4 shows the switching state for the conventional multilevel inverter.

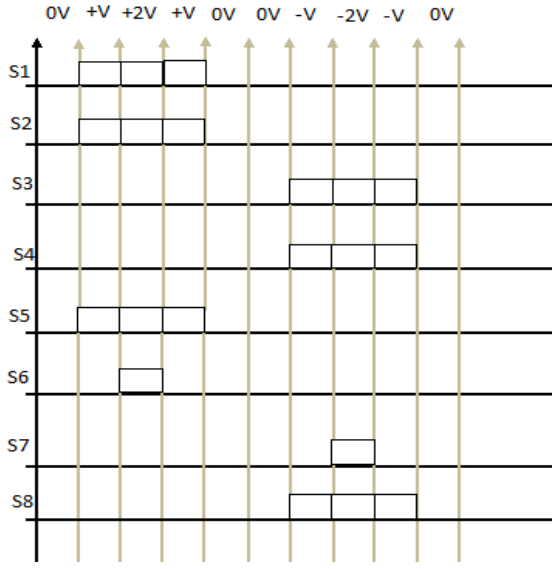

Figure-4. Switching states of .PWM multilevel inverter.

2.3 Cascaded digital control multilevel inverter

The two sides of driver [3] control are active-low and active-high control. In active-low control the FET is closed when the control signal is low or 0, and the FET remains open when the signal is high or 1.In active-high control the control signal is reverse phenomenon. Similarly when the control is used in H-Bridge along with two switches working in active-low and active-High control the opening and closing of the switch depends upon the PWM signal along with the Enable signal, suppose the enable signal is high the circuit remains open and it will not conduct.

The digital control [4] uses 4 flip flops as shown in Figure-5. they are JK flip flop1,JK flip flop2,JK flip flop3,JK flip flop4 and the outputs are (Q1,Q1'),(Q2,Q2'),(Q3,Q3'),(Q4,Q4'). The flip- flops generally are clock edge triggered instead of level triggered, the flip flops are given a clock signal and the input for the JK flip flop1 is given through the constant as 1.The technique is similar to counter and in this process to obatin a seven level output the requirement is n+2 bit counters. The output of JK flip flop1 and JK flip flop2 are made to operate in the first half cycle of the positive cycle and in opposite in the second half of the positive cycle. During the first half of the cycle it acts as a up counter as the steps starts on increasing are done by Q3' in the second half of the cycle it acts as a down counter as the steps starts on decreasing are done by Q3.Q4 and Q4' has been used as the control bits and they are also used to separate the positive and negative switches.

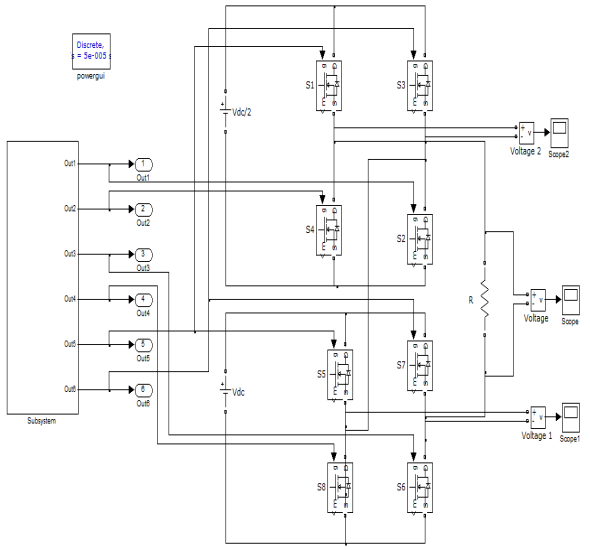

Figure-5. Digital control in multilevel inverter.

In the proposed approach two dc sources were used namely V_{dc} and $V_{dc}/2$, but MATLAB doesn't support counter directly ,hence JK flip flops are used and the output of flipflop is applied to the AND or OR gates inorder to generate the necessary gating pattern. The output of logic gates is Boolean so inorder to convert Boolean to double data conversion block is used. The rationale behind to use double as the conversion type is IGBT devices accept firing signals only in the form of double. The Figure-6 shows the firing circuit with three different sections counter section, logic circuit and pulse separation. The counter counts from 0000 to 1111. Q3 and Q4 are used as control bits for the logic circuit and pulse separation between positive and negative pulses the various switching pattern in the circuit is given in Table-2.

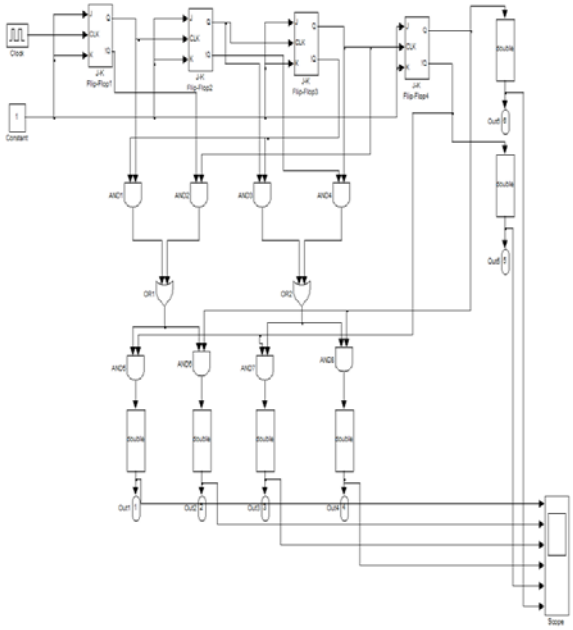

Figure-6. Gate signal generator for digital control multilevel inverter.

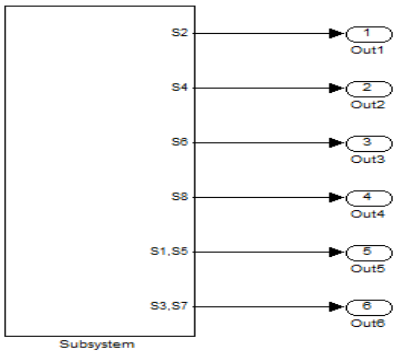

Figure-7. Firing sequence.

Table-2. Conduction table for cascaded digital control in multilevel inverter.

Switch/ volts	S1	S2	S3	S4	S5	S6	S7	S8
30V	1	1	0	0	1	1	0	0
20V	0	0	0	0	1	1	0	0
10V	1	1	0	0	0	0	0	0
-10V	0	0	1	1	0	0	0	0
-20V	0	0	0	0	0	0	1	1
-30V	0	0	1	1	0	0	1	1

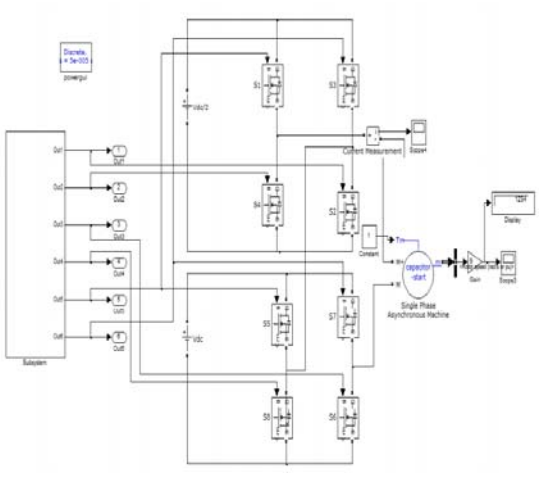

Figure-8. Digital control with motor load.

Figure-8 shows the digital control technique with a motor load [5].

3. RESULTS AND DISCUSSIONS

The simulation results are obtained from MATLAB/SIMULINK.

The simulation results of the output are shown in Figure-11 which uses switches S1, S2, S3, S4, S5, S6, S7 and S8, the input of 1st H-bridge and 2nd bridge combine together to produce five level output. The Figure-9.Shows the conventional PWM cascaded multilevel inverter.

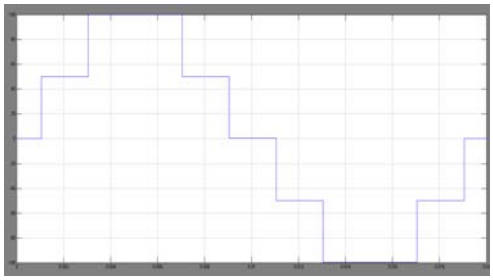

Figure-9. Output of PWM cascaded multilevel inverter.

The THD level of the PWD cascaded multilevel inverter is obtained using the FFT analysis.The THD level is found to be 30.18%, which is shown in Figure-10.

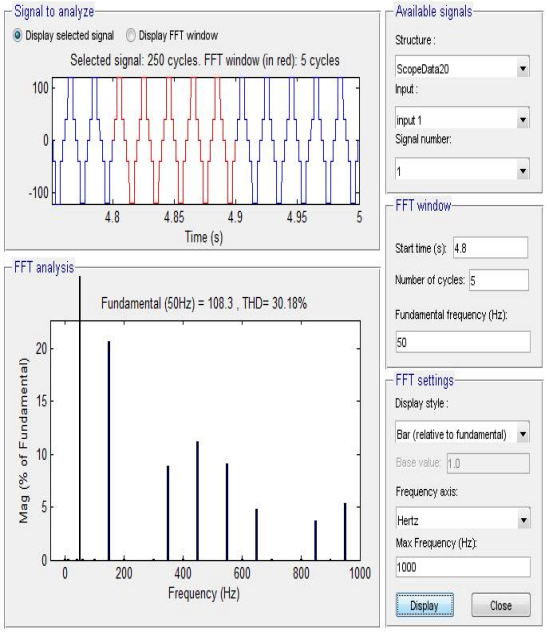

Figure-10.FFT analysis of PWM cascaded multilevel inverter.

The gate pattern for the digital control technique is shown below for switches S1, S2, S3, S4, S5, S6, S7 and S8 from Figures 11(a) to 11(e).

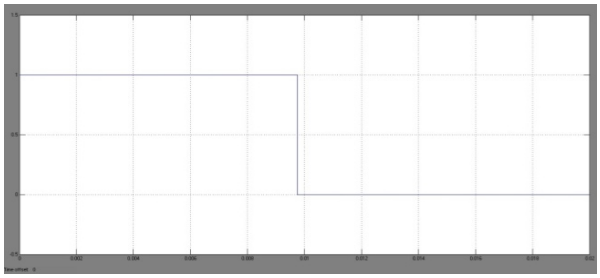

Figure-11(a). Gating pattern of switch S1,S5.

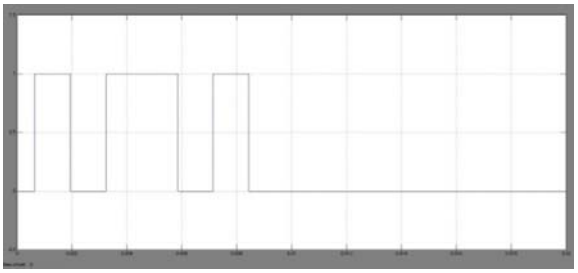

Figure-11(b). Gating pattern of Switch S2.

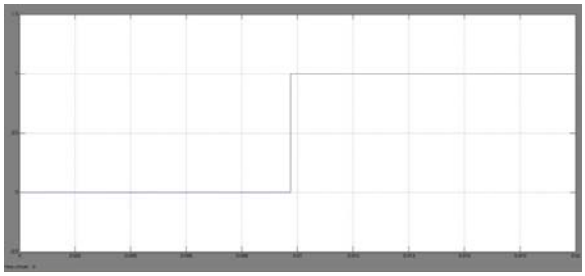

Figure-11(c). Gating pattern of switch S3,S7.

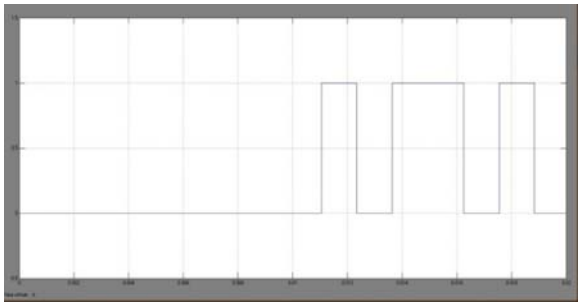

Figure-11(d). Gating pattern of switch S4.

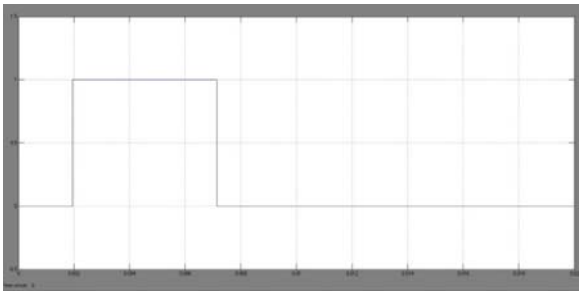

Figure-11(e). Gating pattern of switch S6.

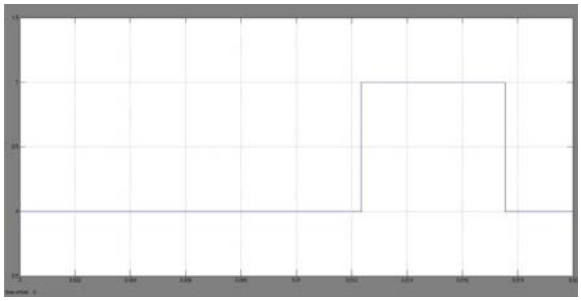

Figure-11(f). Gating pattern of switch S8.

The output of digital control of cascaded multilevel inverter is shown in Figure-12. The THD level of Digital control cascaded multilevel inverter is obtained by using the FFT analysis. The THD[8] level is found to be 14.32% is shown in Figure-13.

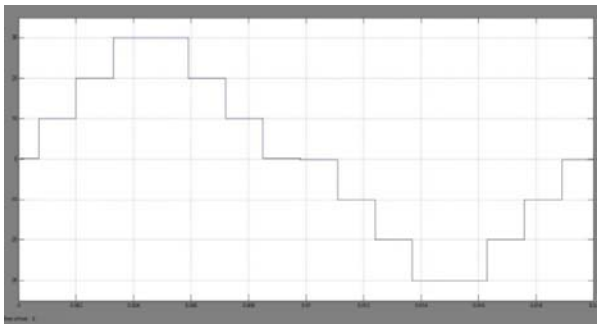

Figure-12. Output of digital control of cascaded multilevel inverter.

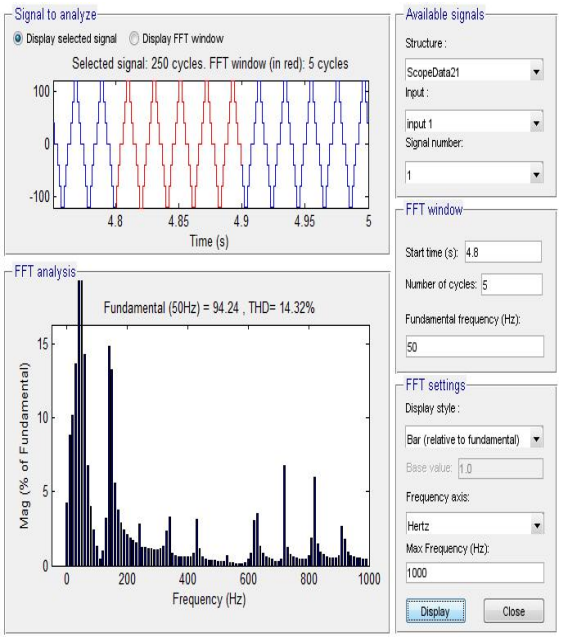

Figure-13.FFT analysis of digital control of multilevel inverter.

The Table-3 gives a comparison .between conventional and proposed method.

Table-3. Conduction table for cascaded digital control in multilevel inverter.

S.No.	Parameters for n sources	Conventional method	Proposed method
1	Number of levels	2n+1	$2^{(n+1)}$-1
2	Number of switches	4n	4n
3	THD(without filter)	20.48%	16.80%
4	Complexity in designing circuit	Complex	simple

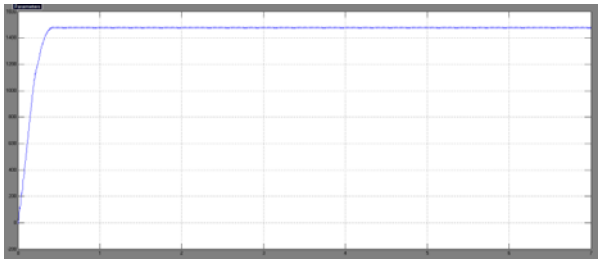

Figure-14. Speed graph of PWM multilevel inverter.

The speed Characteristics of the PWM inverter is shown in Figure-14 and that of the digital approach is shown in Figure-15, the speed of the PWM inverter fed motor runs faster than that of the digital control but the input to digital is very smooth so that the life of the motor is better compared to that of the PWM and speed variation is smooth in digital in comparison with PWM inverter. The experimental set up is shown in Figure-16 and the results are shown in Figure-17 respectively.

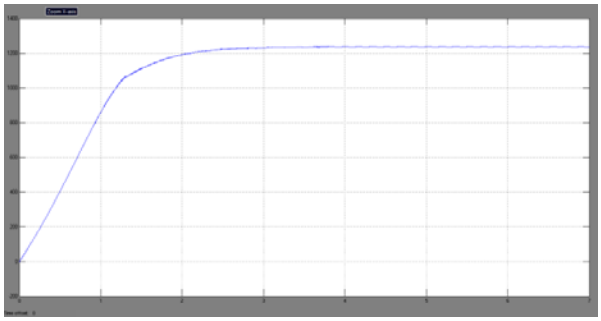

Figure-15. Speed characteristics of digital control multilevel inverter.

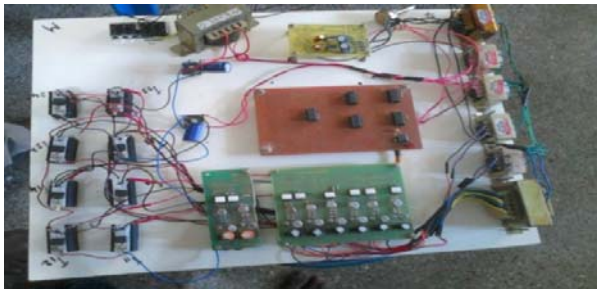

Figure-16. Hardware setup.

Figure-17. Experimental results.

4. CONCLUSIONS

Thus the digital switching approach is employed and the advantage of using digital scheme is that it reduces the uneven degradation of power switches, switching losses when compared to the conventional PWM technique and harmonics are reduced. From the THD analysis the conventional inverter produces a THD of 30.18% whereas the digital control technique produces a THD of 14.32% also the output level has been noted that a seven level output is obtained by increasing the number of stages and its efficiency is also increased. The output results are verified using both by simulation and experimental setup.

REFERENCES

Leon M. Tolbert, Fang Zhen Pengand Thomas G. Habetler. 1999. Multilevel Converter for Large Electric Drives. IEEE transactions on industry applications. 35(1).

José Rodríguez,Jih-Sheng Lai,ZhengPeng. 2002. Multilevel Inverters: A Survey of Topologies, Controls, and Applications.IEEE transactions on industrial electronics. 49(4).

Zhong Du, Leon M. Tolbert, BurakOzpineci, and John N. Chiasson. 2009. Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter. IEEE transactions on power electronics. 24(1).

C.Kiruthika, T.Ambika, Dr.R.Seyezhai. 2012. Implementation of digital control strategy for asymmetric

cascaded multilevel inverter. 2012 International Conference on Computing, Electronics and Electrical Technologies [ICCEET].

Sujitha.N and Ramani.K. 2012. A new hybrid cascaded H-bridge multilevel inverter-performance analysis. IEEE-International Conference on Advances in Engineering, Science and Management (lCAESM -2012).

S.Albert Alexander, T.Manigandan, N.Senthilnathan. 2009. Digital Switching Scheme for Cascaded Multilevel Inverters. Third International Conference on Power Systems, Kharagpur, India.

Jose Rodriguez,Steffen Bernet and BinWu. 2007. Multilevel voltage source converter topologies for Industrial medium voltage Drives.IEEE Transactions on Industrial Electronics. 54(6): 2930-2945.

Yu Liu, Hoon Hong and Alex Q. Huang. 2009. Real time calculation of switching angles minimizing THD for multilevel inverters with step modulation. IEEE Transactions on Induatrial Electronics. 56(6): 285-293.