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MULTILEVEL INVERTER BASED ON LEVEL SWITCH AND H-BRIDGE

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ABSTRACT

This article proposes a topology for construction of multilevel inverter consisting of H-bridge and level switch. In accordance with the proposed topology H-bridge inverts voltage and a switch enables to get any number of voltage levels. At that, in comparison with analogues, the above mentioned topology allows saving on expensive power keys. Moreover, a special technique has been developed to set time of level switching. 13-level inverter has been developed following the proposed topology and methodology. The article highlights the results of simulation in Matlab and an experimental inverter unit.

Keywords: multilevel inverter, inverter topology, switching angles, THD.

INTRODUCTION

In modern power electronics multilevel inverter development got a short in the arm with the appearance of powerful IGBT modules. There are many different methods for multilevel inverter construction. Most of them are described in details in [1, 2]. The simplest multilevel inverter topology is called “Cascaded H-bridge” [3-5]. It consists of several H-bridges in series which is not economically beneficial because IGBT modules are rather expensive. There is an improved topology with less power elements [5, 6]. Diode clamped inverters or [7, 8] flying capacitors [9] are also widely used. The topology highlighted in the article [10] reduces a number of IGBT used but such a topology requires more total supply voltage and a complicated control system. The article proposes construction topology for multilevel inverter combining H-bridge and level switch. At that, the level switch enables to have any number of voltage levels at the inverter output. There is also a methodology presented to determine the switching time of inverter stages. It is based on the geometrical approximation of voltage step curve to sinusoidal wave.

METHODOLOGY FOR DETERMINING THE SWITCHING TIME OF INVERTER STAGES

There are many ways to find switching time of inverter voltage levels. Varieties of Shifting PWM [1, 2, 3] are most often used. All of them are intended to approximate step output voltage of inverter to sinusoidal one and reduce its harmonic components. However, it is not considered that such parameters of inverter output voltage as frequency, amplitude and effective value should conform to the parameters of industrial voltage. To achieve this, the situation, when the areas limited by voltage curves for each stage will be respectively equal, is proper (Figure-1).

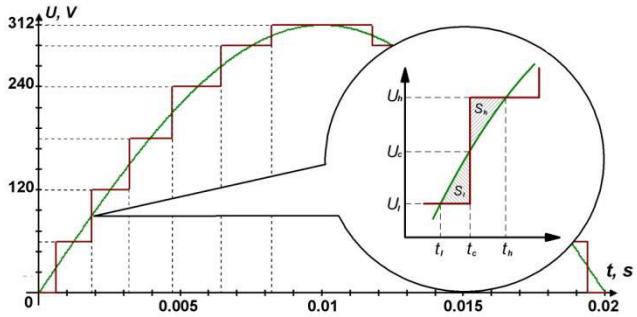

Figure-1. Finding switching time of inverter voltage levels.

Use the following rule [11] to find the areas of such figures. If a continuous function $f(x)$ more or equal to a continuous function $g(x)$ on the interval $[a, b]$, then the area of the figure S, limited by the graphs of the given functions and straight lines $x = a$, $x = b$, can be found by using the following formula

$$S = \int_a^b \big(f(x) - g(x)\big)\, dx. \quad (1)$$

Limits of integrating will be determined as these are the time when sinusoidal voltage equals a certain level. Thus, this time should be calculated according to the formula 2.

$$t = \frac{\sin^{-1}\frac{U}{A}}{2\pi f}. \quad (2)$$

In this expression A is an amplitude of sinusoidal voltage, U - amplitude of level, f - frequency. Thus, areas of the figures can be found by using the following formula

$$S_l = \int_{\frac{\sin^{-1}\frac{U_l}{A}}{2\pi f}}^{t_c} (A \sin 2\pi f t - U_l) dt, \quad (3)$$

$$S_h = \int_{t_c}^{\frac{\sin^{-1}\frac{U_h}{A}}{2\pi f}} (U_h - A\sin 2\pi f t)dt. \quad (4)$$

The unknown time of switching t_c falls within the limits of integrating the given expressions. It is necessary to extract integrals and make $S_l = S_h$. As a result we get the following

$$t_c = \frac{U_h \sin^{-1}\frac{U_h}{A} - U_l \sin^{-1}\frac{U_l}{A} + A\cos\left(\sin^{-1}\frac{U_h}{A}\right) - A\cos\left(\sin^{-1}\frac{U_l}{A}\right)}{2\pi f(U_h - U_l)}. \quad (5)$$

Thus, the formula has been obtained to find the switching time of a certain voltage level.

SIMULATION AND EXPERIMENTAL RESULTS

In accordance with this formula we make a practical calculation for a 13-level inverter. The inverter topology is shown in Figure 2. Since the voltage will be produced by 12 V accumulator batteries in series the voltage levels should be divisible by 12. In this case they are equal to 60, 120, 180, 240, 288 and 312 V respectively. The obtained data are summarized in the Table-1.

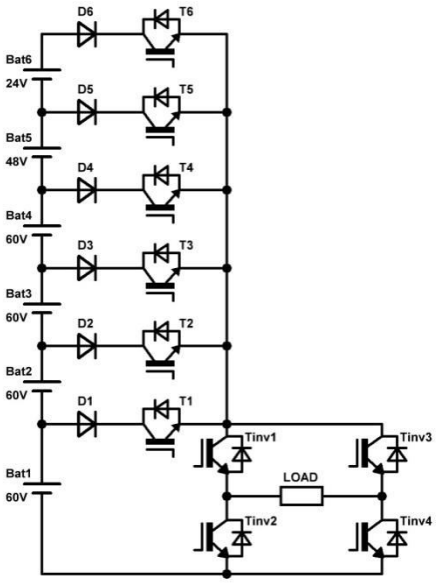

Figure-2. 13-levels inverter circuit.

Table-1. Switching angles in 13-level inverter.

Level	Voltage, V	Switching time, s	Switching angles, deg
1	60	$0.307\cdot10^{-3}$ - $9.693\cdot10^{-3}$	5.526° - 174.474°
2	120	$0.933\cdot10^{-3}$ - $9.067\cdot10^{-3}$	16.794° - 163.206°
3	180	$1.6\cdot10^{-3}$ - $8.4\cdot10^{-3}$	28.8° - 151.2°
4	240	$2.359\cdot10^{-3}$ - $7.641\cdot10^{-3}$	42.462° - 137.538°
5	288	$3.229\cdot10^{-3}$ - $6.771\cdot10^{-3}$	58.122° - 121.878°
6	312	$4.164\cdot10^{-3}$ - $5.836\cdot10^{-3}$	74.952° - 105.048°

A six-level inverter has been simulated based on the obtained results in Matlab software environment (Figure-3). The parameters of inverter output voltage and its harmonic composition were studied with the help of powergui block.

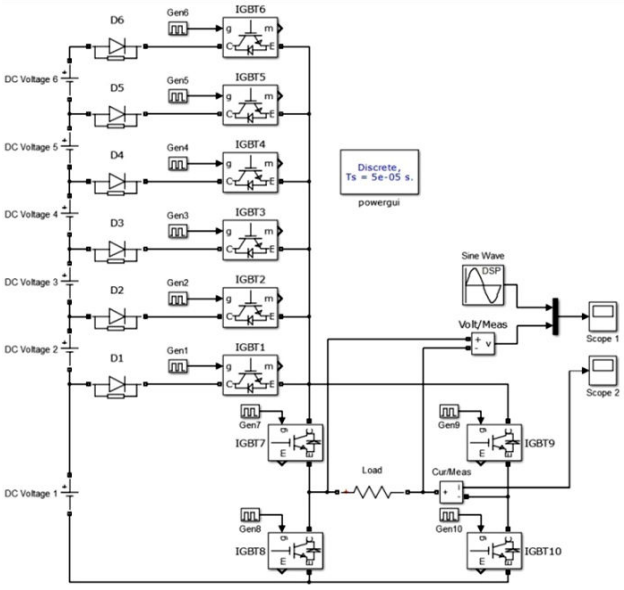

Figure-3. 13-levels inverter model.

The result of simulation is step voltage generation at the inverter output. At 311.5 V amplitude an average square value equals 220.2 V. The ratio of harmonic distortion is 5.17% only which is a good result. For example, the analogues ratio for 13-level inverter in [12, 13] according to HES-PSO-strategy is 6.11%. It has to be recognized that in [14] THD less than 5% has been obtained by using genetic algorithm. However, it should be noted that in this case up to with respect to others shown up 25th and 27th harmonics. They can easily be eliminated by LC-filter.

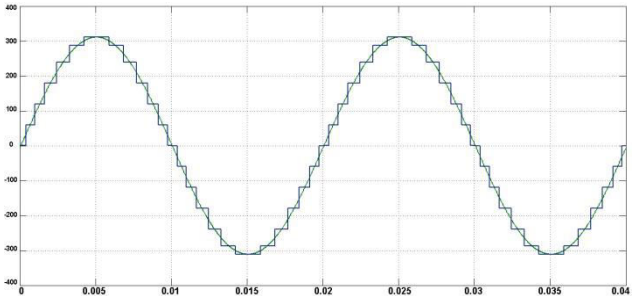

Figure-4. Simulation with MATLAB SIMULINK: output voltage waveform of the 13-levels inverter.

After the scheme validation in MATLAB an experimental unit was assembled. The Figure-5 shows a structural scheme of inverter and the Figure-6 an experimental unit. The inverter consists of a 6-channel switch, a H-bridge and a control system built on microcontroller ATmega32A.

H-bridge is made on the basis of intellectual power module Mitsubishi PM75CLA120. It consists of control impulse amplifier and protection scheme against short circuit, current overload, low voltage or module high temperature. In addition, it produces the "Emergency" signal which is displayed by LEDs HL1, HL2 and HL3. To ensure normal operation the module is optically coupled. The module is powered from the DC source with voltage of +15 V. The nominal power of the developed 13-level inverter is 5 kWt.

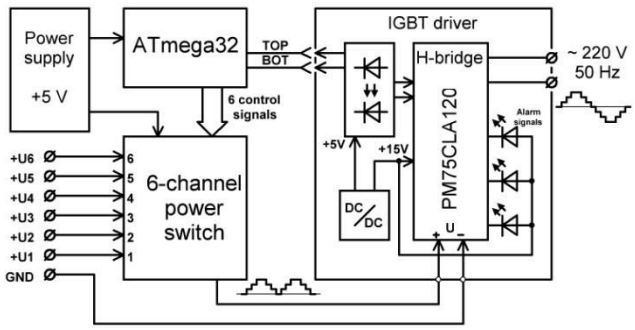

Figure-5. Block diagram of the experimental unit.

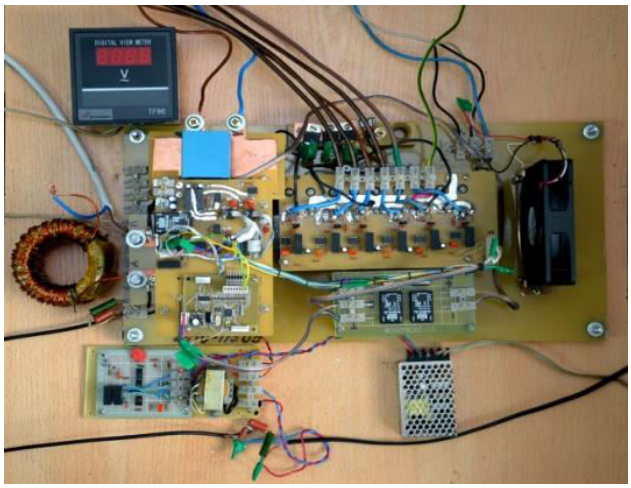

Figure-6. Photograph of the experimental setup.

Figure-7 shows an oscillogram of sinusoid shaped output voltage of the inverter constructed according to the switching angels in Table-1. This oscillogram also shows voltage of industrial network of Almaty City for comparison. As it can be noted the form of multilevel inverter output voltage is more like sinusoidal than the form of voltage in the industrial network.

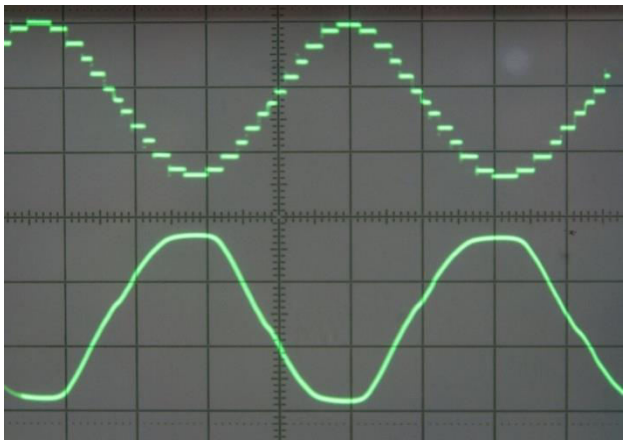

Figure-7. Oscillogram of the 13-level inverter output voltage.

CONCLUSIONS

This article proposed an alternative construction topology for multilevel inverter. The topology can be used to generate voltage of any number of levels. There was a methodology for setting the switching time of levels and a formula for quick calculation proposed. The 13-level inverter was developed according to the proposed topology and methodology for calculation of the switching time which is rather good in relation to the THD and price. The THD of the presented 13-level inverter turned out to be less than the THD of analogue ones. The article presents the scheme of constriction, simulation results and the inverter experimental unit with the capacity of 5 kWt.

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