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ZVS IMPLEMENTATION IN INTERLEAVED BOOST RECTIFIER

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ABSTRACT

This paper presents the implementation of zero voltage switching technique in an interleaved boost rectifier circuit. This converter circuit uses a parasitic capacitor of the MOSFET switch to bring the voltage across the switch to zero. For this purpose, an auxiliary circuit has been provided consisting of two switches and a LC tank circuit. The main application for the converter includes high voltage battery charging in electric vehicles. A comparison of efficiency has been made between conventional interleaved and interleaved resonant circuit to show the performance improvement of the proposed circuit.

Keywords: interleaved boost converter, zero voltage switching, ac/dc converter, power factor correction.

Nomenclature

i_{LA}	Current of Boost inductor 'A'
i_{LB}	Current of Boost inductor 'B'
i_{SA1}	Current through switch 'S_{A1}'
i_0	Output current
I_P	Boost inductor peak current
I_V	Boost inductor valley current
t	time
t_d	Dead time
v_{in}	Input voltage
v_{aux}	Voltage across auxiliary circuit
I_{aux}	Current through auxiliary circuit
v_o	DC output voltage
P_{in}	Input power
P_{swM}	MOSFET switching losses
P_{swD}	Diode switching losses
E_{onM}	MOSFET switch-on energy
E_{offM}	MOSFET switch-off energy
E_{onMrr}	MOSFET reverse recovery energy
U_{DS}	Drain-source voltage
U_{D0}	Drain on state zero-current voltage
U_{DS}	Drain-source voltage
i_D	Drain current
i_F	Current through the diode
tri	Current rise time
tru	Current fall time
tfi	Voltage rise time
tfu	Voltage fall time

INTRODUCTION

The world is moving towards the use of clean and green energy, as a result of which electric vehicles comes into the picture. These electric vehicles make use of high voltage batteries, which could be charged by an AC-DC boost converter [1]-[3].

An interleaved boost converter consists of two switches to reduce the stress across the switch by making the switches to trigger at 180^0 phase shift. Figure-1 shows an AC-DC interleaved [4]-[5] boost schematic.

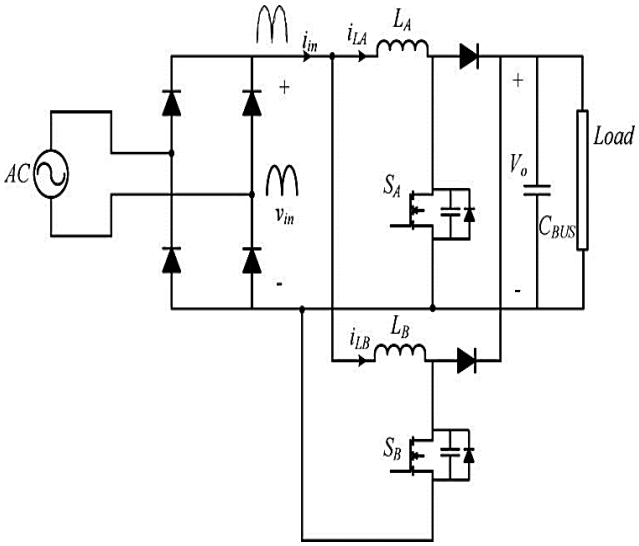

Figure-1. AC/DC interleaved boost schematic.

The power converters suffer from the switching losses due to hard turn on of the switches. This can be overcome by the technique of soft switching wherein, any one of the parameter i.e., either the voltage or the current is brought down to zero. This method reduces the power loss across the switch to zero or negligible.

Different topologies of auxiliary circuits have been presented [6]-[7] to attain soft switching. Figure-2 shows the placement of an auxiliary circuit in a power converter. In the technique of Zero Voltage Switching (ZVS), the voltage across the switch is brought down to zero with the help of parasitic capacitor which is in-built in the switch. The auxiliary circuit provides a path for charging and discharging these capacitors to achieve ZVS.

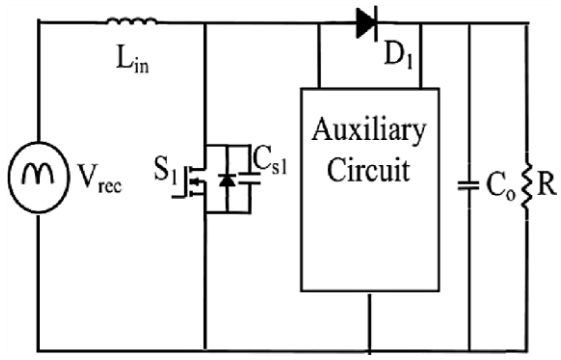

Figure-2. Auxiliary circuit in boost PFC rectifier.

It is always recommended to make the circuit work in critical conduction mode but it has its own downsides as the power handling capability of the circuit may go down. The use of coupled inductor [8]-[10] may also be beneficial but it increases the design and complexity of the circuit.

The front end of an AC-DC boost converter [11]-[13] has a bridge rectifier which might result in significant amount of loss due to the presence of diodes. These losses could be minimized by using silicon carbide diode which is currently preferred diodes for industrial applications.

In this work, ZVS implementation of interleaved boost rectifier is carried out. For this purpose, an auxiliary circuit has been provided which consists of two switches S_{A2}, S_{B2} and a LC tank circuit. A comparison of efficiency has been made between conventional interleaved and interleaved resonant circuit to show the performance improvement of the proposed circuit.

CIRCUIT ANALYSIS OF ZVS INTERLEAVED BOOST CONVERTER

Figure-3 shows the interleaved ZVS boost converter. The switches S_{A1} and S_{B1} are the main switches, i.e., these switches helps in boosting action and the switches S_{A2} and S_{B2} helps in achieving ZVS. The auxiliary circuit [14]-[17] has a LC tank circuit.

Figure-4 shows the theoretical waveforms of the proposed converter which has eight modes of operation as explained below:

Mode I ($t_0 < t < t_1$): As soon as the drain source voltage across the switch S_{A1} comes to zero, a gate pulse is given to S_{A1}. As S_{A1} and S_{B1} are conducting, voltage across the auxiliary circuit will be zero and a constant current will be flowing through the inductor L_{aux}. This mode ends when gate source voltage of S_{B1} is zero. The current through switch S_{A1},

$$i_{SA1}(t) = I_V - I_{aux,p} - \frac{v_{in}}{L_A}(t - t_0) \quad (1)$$

The two phases have 180^0 phase shift; therefore the value of t_1 is given by:

$$t_1 - t_0 = (D - 0.5)T_s \quad (2)$$

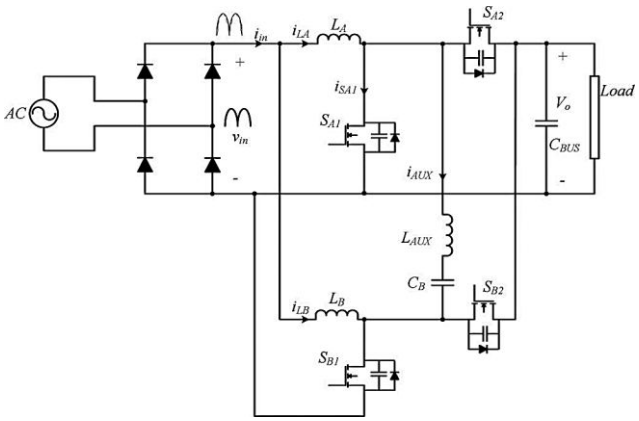

Figure-3. Proposed ZVS interleaved boost rectifier circuit.

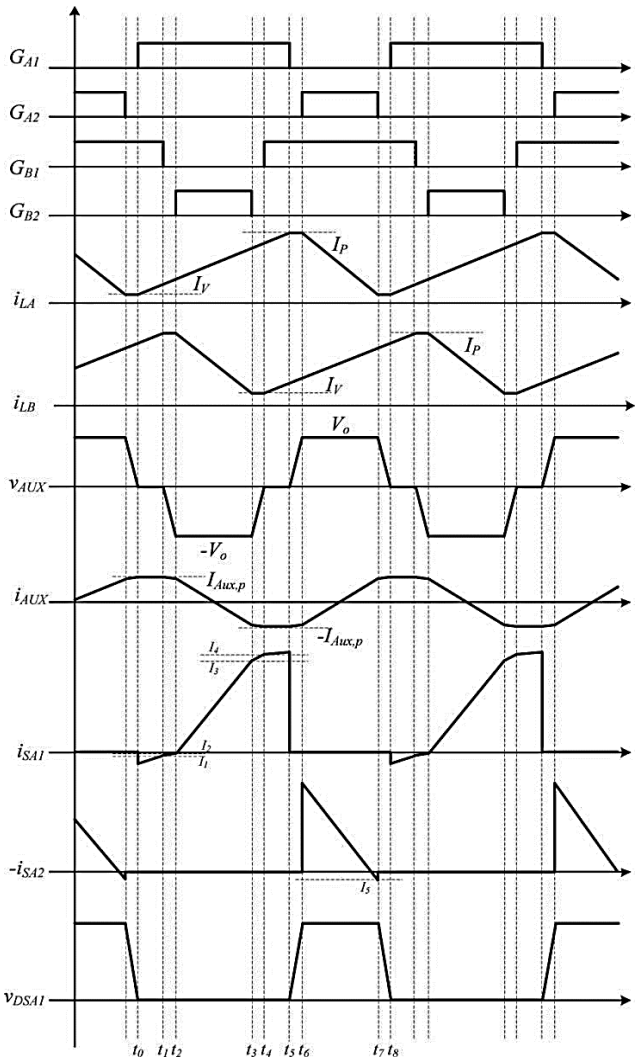

Figure-4. Waveforms of the converter for D >0.5.

Therefore, the duty ratio is given by:

$$D = (t_1 - t_0)f_s + \frac{1}{2} \quad (3)$$

Substituting (2) in (1), the switch current is calculated at t_1 as

$$I_1 = I_V - I_{aux,p}(t) - \frac{v_{in}}{2L_A f_s} - \frac{v_{in}^2}{L_A f_s v_0} \quad (4)$$

Mode II (t_1 <t <t_2): This mode has the dead time between switches S_{B1} and S_{B2}. The capacitor across the S_{B1} will charge to -Vo and the capacitor voltage across the switch S_{B2} is discharges. The current through the boost inductor L_B remains constant. The mode ends as soon as switch S_{B2} is made ON.

$$i_{SA1}(t) = I_V - I_{aux,p} - \frac{v_{in}}{L_A}(t - t_0) + \frac{v_0}{2t_d L_{aux}}(t - t_1)^2 \quad (5)$$

Mode III (t_2 <t <t_3): This mode begins when the charging and discharging of the capacitors of S_{B1} and S_{B2} is completed. Switch S_{B2} is turned ON achieving ZVS. The current through the boost inductor L_B will be decreasing and the voltage across the auxiliary inductor is constant at -Vo. The mode ends when the gate source voltage switch S_{B2} is zero. The current through switch S_{A1} is

$$i_{SA1}(t) = I_V - I_{aux,p} - \frac{v_{in}}{L_A}(t - t_0) + \frac{v_0}{2L_{aux}}t_d + \frac{v_0}{L_{aux}}(t - t_2) \quad (6)$$

Mode IV (t_3 <t <t_4): The mode shows the dead time created between S_{B1} and S_{B2}. The capacitor across the S_{B1} will be discharging from Vo to zero and the capacitor across the S_{B2} will be charging from zero to Vo. This mode ends as soon as the switch S_{B1} is made ON at zero voltage. The current through the switch S_{A1} is given by

$$i_{SA1}(t) = I_V - I_{aux,p} - \frac{v_{in}}{L_A}(t - t_0) + \frac{v_0}{2L_{aux}}t_d + \frac{v_0}{L_{aux}}(t - t_2) \quad (7)$$

Mode V (t_4 <t <t_5): Mode V is same as the mode I. When the gate source voltage is applied to S_{B1}, it starts conducting and it is switched ON under ZVS. Both the main switches will be in ON state to charge the boost inductors. The mode ends when switch S_{A1} is made off and its current through S_{A1} given as:

$$i_{SA1}(t) = I_V + I_{aux,p} - \frac{v_{in}}{f_s L_A}D \quad (8)$$

Mode VI (t_5 <t <t_6): A dead time between S_{A1} and S_{A2} has been created to switch ON S_{A2} at zero voltage. The capacitor across the switch S_{A1} is charging from zero till Vo and that of S_{A2} is discharging from zero to -Vo.

Mode VII (t_6 <t <t_7): The switch S_{A2} is made ON and the current flows from source to load. The voltage across the auxiliary circuit is constant.

Mode VIII (t_7 <t<t_8): This mode is the dead time between switches S_{A1} and S_{A2} and the mode I continues.

DESIGN OF AUXILIARY INDUCTOR

The auxiliary inductor has been designed such that it could charge and discharge the capacitors across the switches. The energy required to charge and discharge the capacitor as well as to neutralize inductor energy is given by:

$$W = \frac{1}{2}L_A\left(\frac{P_{in}}{v_{in}} - \frac{v_{in}(1-(v_{in}/v_0))}{2L_A f_s}\right)^2 + C_{so}v_0^2 \quad (9)$$

The energy present in auxiliary inductor should be greater or equal to the energy derived in equation (9). Therefore, we have

$$\frac{1}{2}L_{aux}I_{aux,p}^2 \geq \frac{1}{2}L_A\left(\frac{P_{in}}{v_{in}} - \frac{v_{in}(1-(v_{in}/v_0))}{2L_A f_s}\right)^2 + C_{so}v_0^2 \quad (10)$$

Hence, the value for auxiliary inductor is given by

$$L_{aux} \leq \frac{\left(v_{in}^2(1-(v_{in}/v_0))^2/4f_s^2\right)}{L_A((P_{in}/v_{in})-(v_{in}(1-v_{in}/v_0))/2L_A f_s))^2+2C_{so}v_0^2} \quad (11)$$

LOSS CALCULATION

Power losses in a power converter can be classified as conduction losses and switching losses:

Conduction losses: The instantaneous value of MOSFET conduction loss is given by:

$$P_{CM}(t) = U_{DS}(t).i_D(t) = R_{DSon}.i_D^2(t) \quad (12)$$

The instantaneous value of diode conduction loss is given by:

$$P_{CD}(t) = U_D(t).i_F(t) = U_{D0}.i_F(t) + R_D.i_F^2(t) \quad (13)$$

Switching losses

a) Switch-on transient

The switch-on energy loss in MOSFET and diode is given as:

$$E_{onM} = \int_0^{tri+tfi} U_{DS}(t).i_D(t).dt = E_{onMi} + E_{onMrr} = U_{DD}I_{Don}\frac{tri+tfu}{2} + Q_{rr}U_{DD} \quad (14)$$

b) Switch-off transient

The switch-off energy loss in MOSFET is given as:

$$E_{offM} = \int_0^{tri+tfi} U_{DS}(t).i_D(t).dt = U_{DD}.I_{Doff}.\frac{tru+tfi}{2} \quad (15)$$

The total switching losses of MOSFET and diode are given as:

$$P_{swM} = \left(E_{onM} + E_{offM}\right).f_{sw} \quad (16)$$

$$P_{swD} = \left(E_{onD} + E_{offD}\right).f_{sw} \approx E_{onD}.f_{sw} \quad (17)$$

HARDWARE RESULTS

The experimental prototype shown in Figure-5 is designed for 50W, where input and output voltages are 50V and 85V respectively. The values of boost inductor, output capacitor and auxiliary inductor are given in Table-1.

Table-1. Converter parameters.

Parameter	Value
Boost Inductor (LA,LB)	270uH
Output Capacitor (CBUS)	470uF
DC Blocking Capacitor	1uF
LAUX	1mH

Figure-6 shows the waveform of the pulses generated for 80kHz switching frequency with a specific dead time for charging and discharging of the capacitors. Figure-7 shows the waveforms of input current (Iin), input voltage (Vin), output voltage and output current, respectively.

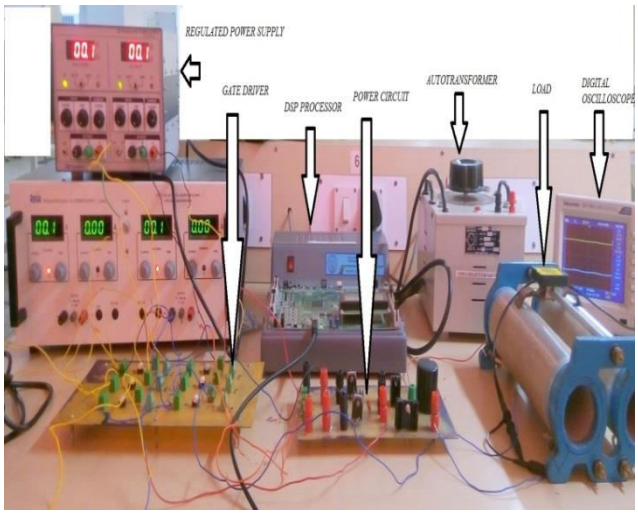

Figure-5. Hardware setup of the proposed converter.

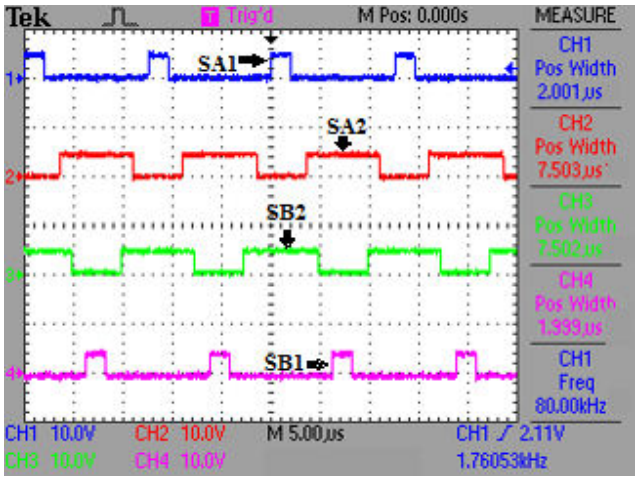

Figure-6. Gate pulses waveforms with dead time.

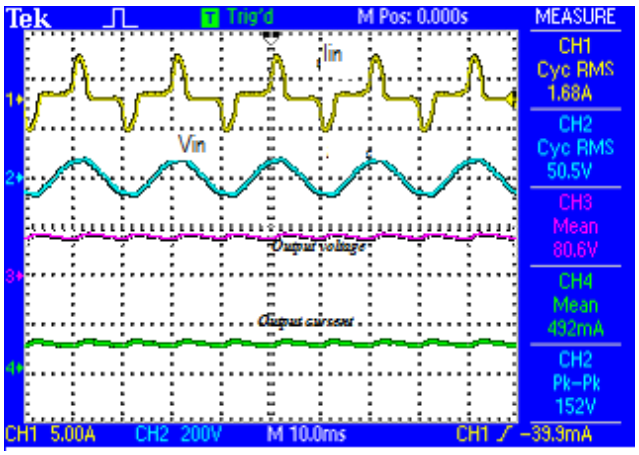

Figure-7. Waveforms of input current (Iin), input voltage (Vin), output voltage and output current.

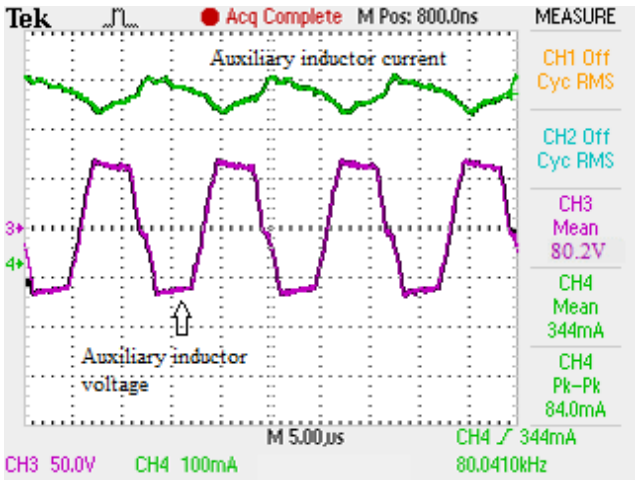

Figure-8. Waveforms of auxiliary inductor voltage and current .

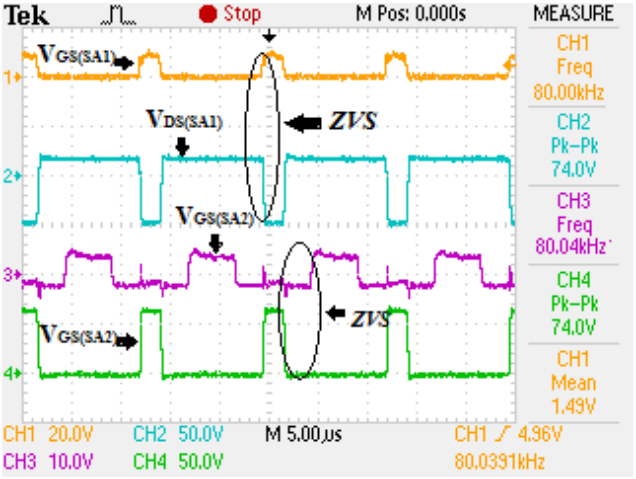

Figure-9. Waveforms of switches S_{A1} and S_{A2} showing ZVS.

Figure-8 gives the current and voltage waveforms of the auxiliary inductor. The inductor current is 0.34A. The voltage across the inductor is 80.2V. Figure-8 shows the gate-source voltage and drain-source voltage of the switches S_{A1} and S_{A2} which shows the ZVS achievement.

The result of the proposed ZVS interleaved boost circuit is compared in terms of efficiency with a traditional interleaved boost circuit. Figure-10 shows the comparison between losses of the interleaved with that of the proposed converter. It is clear that the losses are reduced by 2% in ZVS boost converter. Hence the efficiency is improved than the conventional topology for various load conditions as shown in Figure-11.

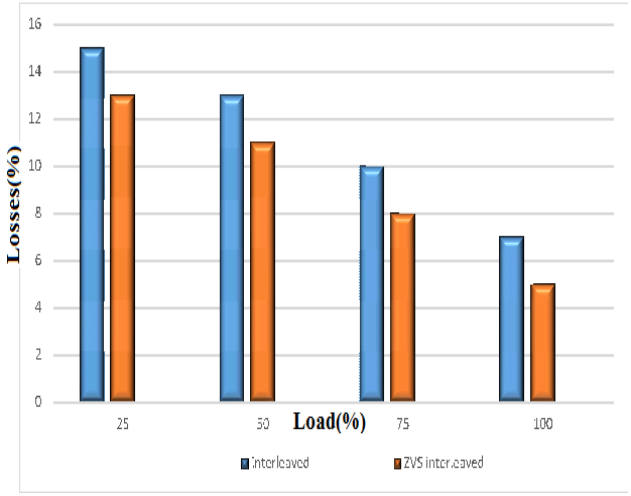

Figure-10. Load (%) Vs Losses (%).

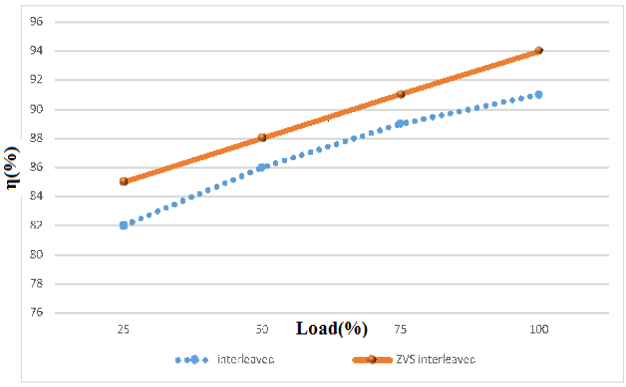

Figure-11. Load (%) Vs η (%).

6. CONCLUSIONS

In this paper, hardware implementation of interleaved boost converter with soft switching for the power MOSFETs, through an auxiliary circuit is discussed. This auxiliary circuit helps in achieving ZVS by providing reactive current during the turn ON and turn OFF of the MOSFETs to charge and discharge the output capacitors of the MOSFETs. The result shows the superior performance of the ZVS interleaved converter compared to the conventional one in terms of efficiency.

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