VOL. 10, NO. 16, SEPTEMBER 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

COMPARATIVE ANALYSIS OF CURRENT DIFFERENCING BUFFER AMPLIFIERS

Sachin Kumar Rajput and Anu Mehra
ECE Dept., ASET, Amity University, Noida, India
E-Mail: skrajput@amity.edu

ABSTRACT

This paper presents comparative analysis of various current differencing buffer amplifiers as an active building block in realization of analog signal processing circuit. The versatility of multi terminal active element (CDBA) as current mode and voltage mode circuit implementation using various methodologies has been reviewed. Also a comparative analysis based on characteristic parameters of various CDBA topologies is done.

Keywords: active element, CDBA, current mode, filter, analog circuit.

INTRODUCTION

The need of the low supply voltage and low power consumption for the electronics circuits leads to the development of microelectronic technologies which are simple, low cost and with minimum number of active and passive elements. Along with power and supply, demand of high speed and accuracy of signal processing, larger band-width also appears in many applications which lead the designer to opt trade-off solutions. Voltage mode circuits, e.g. classical Op-Amp, serves as the main building block in analog signal processing circuits like filters, oscillator, etc. Due to closed loop voltage gain, conventional Op-Amp shows band-width limitation. A potential substitute to surmount this problem is current mode circuits. AD844, the current feedback Op-Amp IC, can be used commercially without suffering from gain bandwidth and slew rate limitations in low frequency range. A trend of evolution of current mode circuits, from CCI (Smith and Sedra, 1968), CCII (Sedra and Smith, 1970), to many different CC blocks, has been observed and adopted in the last few decade. Current mode circuits can be used for low supply, low power, high slew rate, low swing, higher bandwidth and better signal linearity and for a variety of signal processing units (Biolek *et al.*, 2008), (Pathak, Singh and Senani, 2014). Prior to 1990, development in current conveyor circuits was reviewed in (Wilson, 1990). Third generation current conveyor (CCIII) was introduced by A. Fabre in 1995(Fabre, 1995). A new versatile, multi-terminal active circuit building block, current differencing buffer amplifier (CDBA) was proposed by Acar and Ozoguz in 1999 (Acar and Ozoguz, 1999). Its flexibility to operate in both voltage and current mode and low parasitic are suitable for wide band applications (Acar and Sedef, 2003), (Ozoguz, Toker and Acar, 1999), (Koksal, Oner and Sagbas, 2009), (Toker *et al.*, 2000). It provides an attractive feature in terms of requirement of less number of passive components and better cascadability for various filter circuit and other analog signal processing circuit implementation. A number of active device are also proposed with modification of CDBA as CCCDBA, ZC-CDBA (Maheshwari and Khan, 2004), (Bashir and Shah, 2012), (Alavbeyolu, Guney and Kuntman, 2013) where the input port resistance is controlled by external bias current.

This paper presents the review on development of various CDBA topologies used in realization of analog signal processing circuits. The II section gives the basic concept of CDBA. The III section presents the various CDBA realization schemes. A comparative analysis is presented in section IV considering the different performance parameter of CDBAs.

CDBA Concept

The circuit symbol of CDBA and its equivalent circuit are given in Fig.1 (a) and Fig.1 (b). Its current and voltage behavior is characterized by the following equations.

$$\begin{pmatrix} i_z \\ v_w \\ v_p \\ v_n \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} v_z \\ i_w \\ i_p \\ i_n \end{pmatrix} \quad (1)$$

From the characteristic equation and Figure-1, p, n are current mode input terminals, z is current mode output while w is the voltage mode output terminal. Ideally, input impedance of p and n terminal is zero and output impedance of w and z are zero and infinite respectively. According the equation (1), difference of input currents (i_p and i_n) is converted into output voltage v_w through the impedance externally connected to the z terminal.

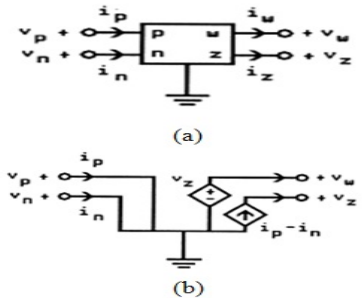

Figure-1. (a) Current Differencing Buffer Amplifier block and (b) Equivalent Circuit (Acar and Ozoguz, 1999).

CDBA REALIZATION SCHEMES

CDBA implementation with CFAs

A multi terminal active component, Current differencing buffered amplifier with two inputs and two outputs is proposed by Acar and Ozoguz (Acar and Ozoguz, 1999). CDBA is realized by using commercially available CFAs, AD844. The realized circuit diagram of this CDBA is shown in Figure-2. CDBA advantages are mainly in the implementation of continuous-time filters.

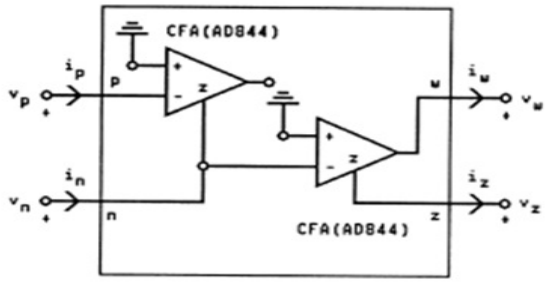

Figure-2. Implementation of CDBA with CFAs (Acar and Ozoguz, 1999).

Taken into account the non-idealities of CDBA, the characteristic equation (1) can be rewritten as $v_p = 0$, $v_n = 0$, $i_z = \alpha_p i_p - \alpha_n i_n$, $v_w = \beta v_z$, Where, α_p, α_n and β represents the current and voltage gains respectively, and can be expressed as α_p=1-εp, α_n =1-εn , β =1-εv, with $|\varepsilon p|<<1$, $|\varepsilon n|<<1$, $|\varepsilon v|<<1$; εp, εn and εv denotes current tracking and voltage tracking errors respectively (Acar and Sedef, 2003).

Realization of CDBA using 3- AD844

Conventional implementation of CDBA with two AD844 has raised a noisy w-terminal voltage output (Acar and Ozoguz, 1999). Due to this reason, a new implementation of CDBA is proposed using three AD844 in Figure-3 (Koksal, Oner and Sagbas, 2009).

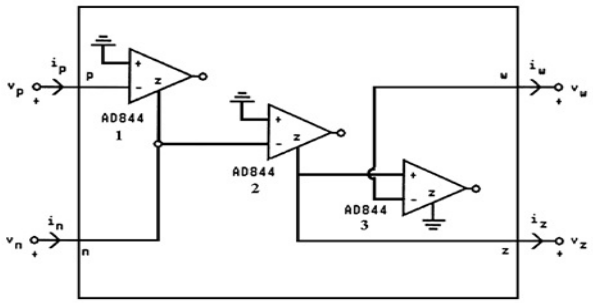

Figure-3. Three-AD844 CDBA Realization (Koksal, Oner and Sagbas, 2009).

This new implementation transfers second AD844- *z* terminal voltage into the *p*-terminal of the third AD844. As $v_p = v_n$, *n*-terminal of the third AD844 is used as noise free *w*-terminal voltage output. Three AD844 CDBA shows good agreement between simulated and experimental results at frequency lesser than 3 MHz but over this frequency range discrepancies arise because of stray capacitances of AD844s which roots affective attenuations at high frequencies.

CMOS Implementation of CDBA

The CDBA block shown in Figure-1 (a) is implemented using CMOS devices by Ozoguz, Toker and Acar in Figure-4 (Ozoguz, Toker and Acar, 1999). CMOS CDBA consisting of a differential current controlled current source (DCCCS) followed by a voltage buffer.

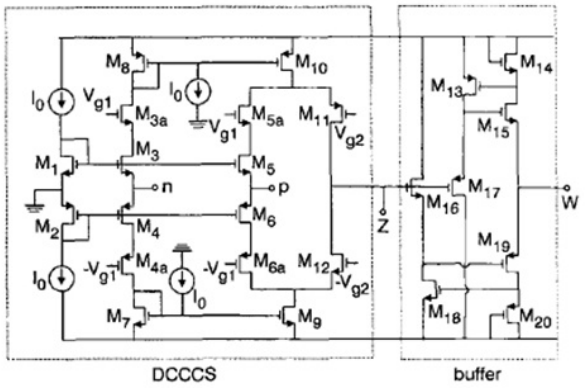

Figure-4. CMOS CDBA Implementation (Ozoguz, Toker and Acar, 1999).

A simplified implementation of CDBA is presented by Toker, Özoˇguz, Çiçekoˇglu, and Acar in Figure-5 (Toker *et al.*, 2000).

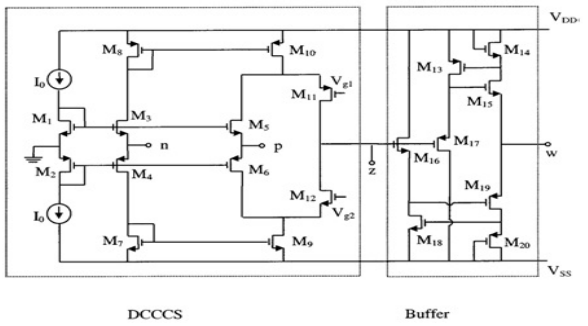

Figure-5. Simplified Implementation of CMOS CDBA (Toker *et al.*, 2000).

In Figure-5, the aspect ratio of the transistor M3(M4) should be twice as large as those of M1(M2) and M5(M6). This circuit can be converted to the well known CFOA by removing the transistor M5 and M6. This shows that CDBA is a less complicated circuit compare to some other current mode active element. CDBA offers the advantages of the CFA and CCII, such as high slew-rate, wide bandwidth and simple implementation.

High Performance CDBA

Tarim and Kuntman presented a current differencing buffer amplifier employing two CCII and a voltage buffer (Tarim and Kuntman, 2001). It is apparent that overall performance is determined by the performance of CCII and voltage buffer blocks. Taking this into account, high performance blocks were chosen to implement the circuit in Figure-6 and Figure-7. It contains only NMOS transistors and is designed to be implemented in CMOS technology. Figure-6 shows the CCII circuit and Figure-7 is the voltage buffer implementation used for realization of CDBA. This voltage buffer circuit offers very low output impedance and low gain error (Palmisano, Paluinbo and Pennisi, 2000).

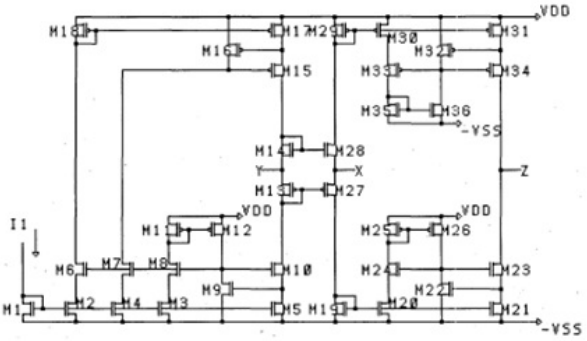

Figure-6. CCII circuit to realize the CDBA (Tarim and Kuntman, 2001).

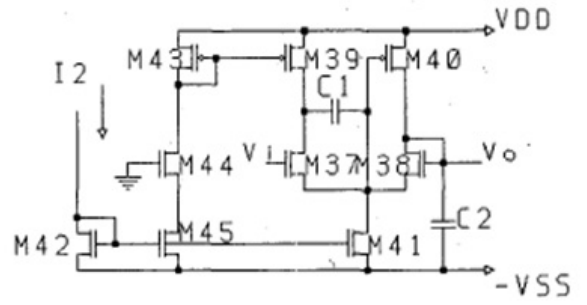

Figure-7. Voltage buffer to realize the CDBA (Tarim and Kuntman, 2001).

Simulation result of this CDBA exhibit the values of current and voltage transfer functions are 0.996 and 0.9999 respectively at low frequencies and 70 MHz and 37 MHz are the -3dB bandwidths respectively. The impedance of *p* and *n* terminal for broad frequency range, have value 645Ω. The *w* terminal impedance has values 49Ω and 1555Ω at low frequency and at 40MHz respectively. Simulation result yields 678 MΩ value of *z* terminal at low frequency and terminal capacitance of 0.2pF.

Low Voltage Operation CDBA in Bipolar Technology

Tangsrira T, Fujii and Surakampontorn proposed a CDBA in low voltage operation (Tangsrirat, Fujii and Surakampontorn, 2002). From (1), the difference of current i_p-i_n, is converted to the output voltage v_w, through an impedance connected at the terminal *z*. A CDBA is basically a combination of a current subtractor (current differencing circuit) and a voltage follower. The proposed low-voltage CDBA in bipolar technology is shown in Fig.8, where low input resistance input stages are functioned by transistors Q1-Q4 and Q7-Ql0 and the buffer stage formed by complementary NPNs and PNPs (Q14-Ql7) which force the *w* terminal to the potential of the *z* terminal. This CDBA is simulated by PSPICE using 0.7µm BiCMOS process parameter with ±1 Volts power supply and bias current *IB* of 200µA which is realized by current mirror circuits. Simulation confirms the cutoff frequencies in the order of hundred MHz with r_z = 1 KΩ and r_w = 10 KΩ.

Low-Voltage NMOS CDBA

CMOS based CDBA shows quite high (of several hundred ohm) terminal resistance (Ozoguz, Toker and Acar, 1999), (Tarim and Kuntman, 2001) and voltage gain, β≈0.7. This limits the CDBA application and need to include methods to compensate these effects. Thus a low supply operated CDBA with low input terminal resistance are the natural choice for analog signal processing circuits. In order to achieve that, a low-voltage CDBA using only NMOS transistors proposed by W. Tangsrirat, K. Klahan, T. Dumawipata and W. Surakampontorn in 2006 (Tangsrirat *et al.* 2006). The proposed CDBA (Figure-9) has low resistance value at both current-input terminal (*p*, *n*) and at the output-voltage terminal (*w*). A low impedance current conveyor (CCII+) is used with some modification for current differencing circuit realization. In the realization of CDBA, a negative current mirror using only NMOS is employed to achieve the high frequency response as signal has an all NMOS signal path. Since the unity gain bandwidth depends on transconductance, an all NMOS path is used due to the superiority of NMOS over PMOS in terms of: (1) For a typical n-well process, unity gain frequency of NMOS devices is approximately twice that of PMOS devices which is due to the higher saturation velocity of electron compared to holes (Abou-Allam *et al.*, 2000), (2) Gate length of PMOS must be three times wider than NMOS to obtain the same transconductance in view of the fact that the junction capacitance per unit area is approximately two times larger for PMOS as that of for NMOS (Steyaert *et al.*, 1995).

The circuit can operate at a low power supply voltage of (2VDSi + VIB), where VIB and VDsi are the voltage drop at the bias current source IB and the drain-to-source voltage of the transistor Mi, respectively and can operate with minimum supply voltage of ±1.25V. With 0.5µm CMOS process, the proposed CDBA simulation results in terminal resistance of n, p and w, ≈13Ω while z terminal value is 290kΩ with -3dB bandwidth of about 500 MHz. The maximum offset current from the terminal p and n to the terminal z is equal to 0.49µA, which is mainly a result of the influence of the current transfer errors from the mismatched mirroring transistors. The current and voltage gains αp, αn and β are found to be 0.991, 0.996 and 0.989, respectively which respectively

corresponds to the errors of 0.99%, 0.4% and 1.11% (Dumawipata, Tangsrirat and Surakampontorn, 2007).

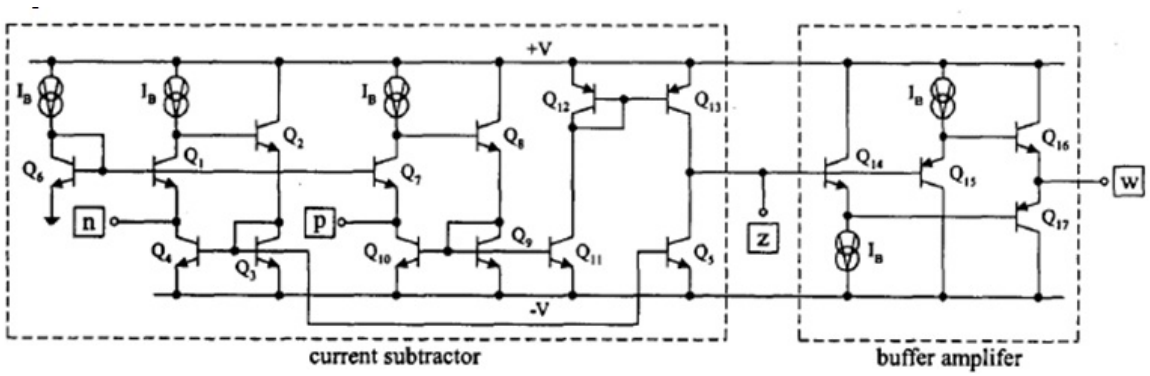

Figure-8. Low Voltage Operation CDBA (Tangsrirat, Fujii and Surakampontorn, 2002).

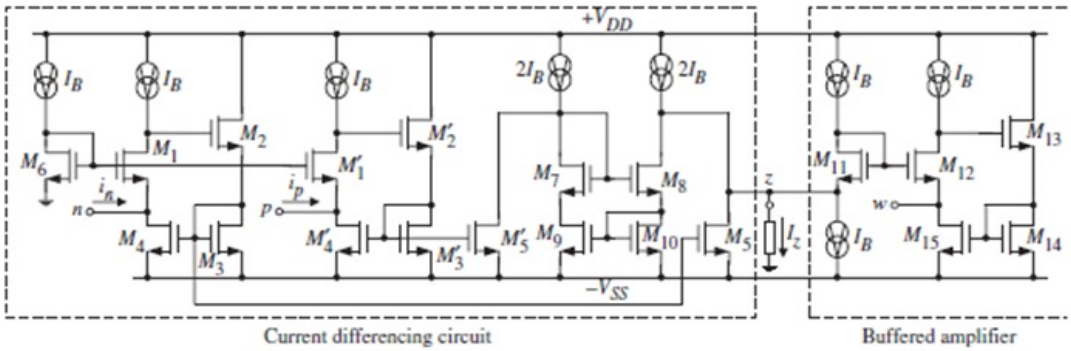

Figure-9: Low-Voltage NMOS CDBA (Tangsrirat *et al.*, 2006).

NPN CDBA

Sawangaroml, Tangsrirat and Surakampontom proposed NPN transistor based CDBA in 2006 (Sawangaroml, Tangsrirat and Surakampontom, 2006). The proposed and designed CDBA can operate with low voltage supply of ±1 volts. In order to achieve the high frequency response, the presented CDBA is designed such that the signal has an all NPN transistor signal path. The circuit in Figure-10, the current differencing block is functioned by two unity gain current amplifiers composed of Q1-Q5 and Q7-Q11in addition with a current mirror by Q12-Q15, whose output current is the difference of i_p and i_n (i_p-i_n). Buffer voltage amplifier block is given by Q16-Q20 which forces the w terminal voltage (v_w) to that of the z terminal (v_z) i.e. $v_w = v_z$. This circuit can operate at low supply voltage as only one current source and two transistors are connected between the positive and negative supply rails. The bias current chosen to 200 µA for the simulation and the cutoff frequencies of i_z/i_p and i_z/i_n are approximately at 126 MHz and 119 MHz, respectively. The simulated frequency response of the voltage transfer between the port z and w (v_w/v_z), with a resistor of 1 kΩ connected from port z to ground, is observed with -3dB frequency of about 200 MHz.

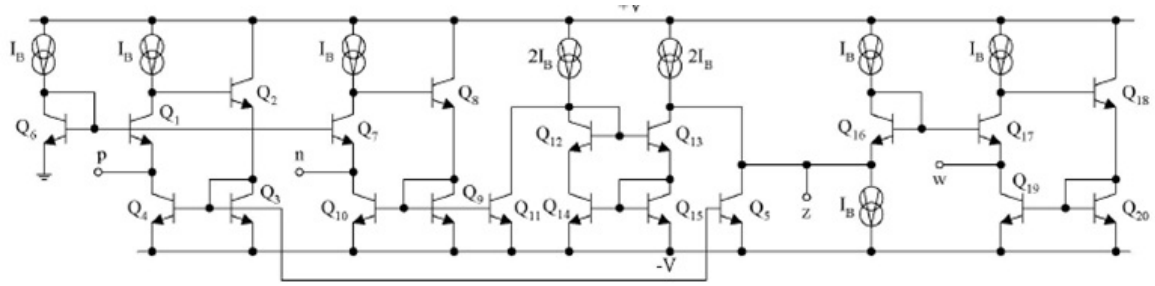

Figure-10. NPN Based CDBA (Sawangaroml, Tangsrirat and Surakampontom, 2006).

Low Power High Performance CDBA

A low power high performance CDBA is proposed by Cakir and Cicekoglu (Cakir and Cicekoglu, 2008). The circuit is realized by current differencing circuit (M1-M10) and voltage buffer (M11-M18) Figure-11. This current differencing circuit is based on the flipped voltage follower current sources (FVFCS) which is responsible for the low input resistance at the input ports. The proposed CDBA operates at V_{SS} = ± 0.75 V. The output stage is designed with a differential FVF (DFVF) topology (Carvajal *et al.*, 2002) based class AB voltage buffer. This stage offers moderate swing and low output impedance. The simulation result shows that the impedance of port *p*, *n*, *z* and *w* are 50 Ω, 50 Ω, 102 kΩ and 158 Ω respectively for wide frequency range with current and voltage gain, α = 0.978 and β = 0.970. The power consumption is 1.2 mW and the offset current at port *z* is 0.14 µA.

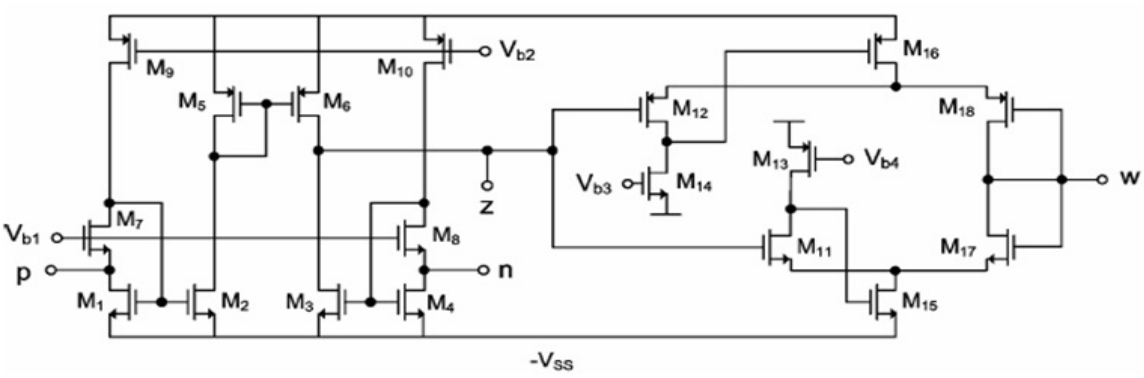

Figure-11: Low Power High Performance CDBA (Cakir and Cicekoglu, 2008).

Low Voltage Low Power CDBA

A low voltage low power CMOS CDBA proposed by Cem Cakir, Shahram Minaei, and Oguzhan Cicekoglu (Cakir, Minaei and Cicekoglu, 2009),(Cakir, Minaei and Cicekoglu, 2010). The CDBA (Figure-12) operates with the minimum supply voltage of VDD = -VSS = 0.6V. Realization of low voltage CDBA circuit is based on the use of combination of current differencing circuit and voltage buffer. This circuit shows better performance by consuming less power as compare to the other CDBA circuits on hand with only 560µW. Offset on terminal-*z* is 0.05µA. The terminals resistance r_p, r_n, r_z and r_w are equal to 56.4Ω, 56.4Ω, 157kΩ and 270Ω respectively. The -3dB bandwidths of the current gains (i_z/i_p) and (i_z/i_n), and the voltage gain (v_w/v_z), are respectively located at 25MHz, 25MHz and 470MHz.

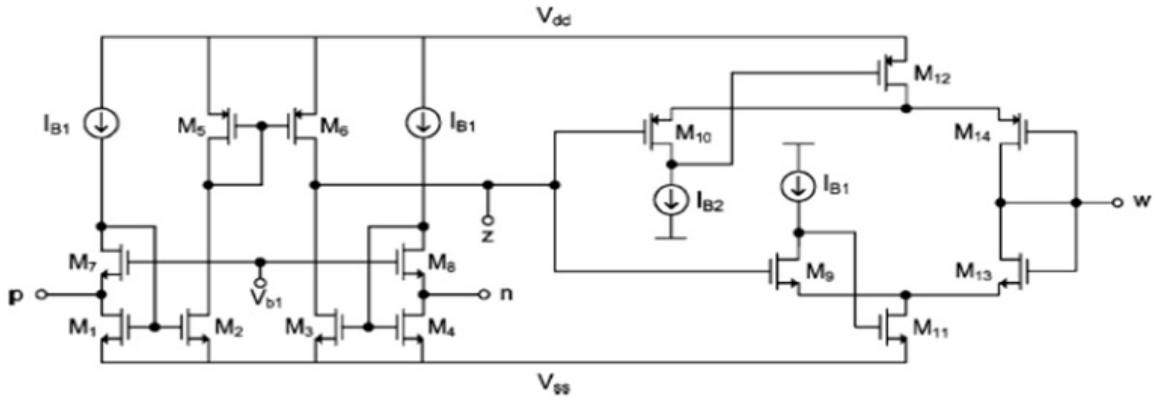

Figure-12. Low Voltage Low Power CDBA (Cakir, Minaei and Cicekoglu, 2010).

Low Voltage Class AB CDBA

In 2011, Arnon Kanjanop and Varakorn Kasemsuwan proposed present a DTMOS based CDBA (Kanjanop and Kasemsuwan, 2011). The class A implementation of CDBA limits the current amplitude and to alleviate this problem is large bias current which leads to large power consumption. To overcome this problem, CDBA is implemented based on two low voltage current mirrors and of value 16.89 Ω, 15.99 Ω, 102.4 kΩ and 15.56 Ω. The current transfer ratio and voltage transfer ratio are found to be i_z/i_p =0.998, i_z/i_n = 0.996 and v_w/v_z =

0.995 with the respective bandwidths of 460, 522 and 172 MHz.

COMPARATIVE ANALYSIS OF CHARACTERISTIC PARAMETERS OF CDBA CIRCUITS

The improvement in performance parameters with the development of CDBA from Table-1 confirms the suitability of this element in various analog signal processing circuits at low voltage. Also the result (Kanjanop and Kasemsuwan, 2011) claims as a suitable candidature for low voltage low power circuits with a wide frequency range.

Table-1. Comparative Analysis of characteristic parameters.

Reference	Operating Supply (volts)	Terminal Impedance				-3dB frequency (MHz)
		p (Ω)	n (Ω)	z (Ω)	W (Ω)	
(Toker et al., 2000)	± 2.5	710	390	NA	NA	NA
(Tarim and Kuntman, 2001)	± 5	645	645	678M	49	70
(Tangsrirat, Fujii and Surakampontorn, 2002)	± 1	NA	NA	1k	10k	100
(Tangsrirat et al., 2006)	± 1.25	≈13	≈13	290k	≈13	500
(Sawangaroml, Tangsrirat and Surakampontorn, 2006)	± 1	NA	NA	NA	NA	200
(Cakir and Cicekoglu, 2008)	± 0.75	50	50	102k	158	NA
(Cakir, Minaei and Cicekoglu, 2009)	± 0.75	46.9	46.9	184	25.1	158
(Cakir, Minaei and Cicekoglu, 2010)	± 0.6	56.4	56.4	157k	270	25
(Kanjanop and Kasemsuwan, 2011)	± 0.7	16.89	15.99	102.4k	15.56	460

CONCLUSIONS

This paper presents a literature review on the current status and the recent development of the current differencing buffer amplifier. The results of various reviewed papers explore and confirm the applicability of CDBA in analog signal processing circuits to mitigate the limitation due to the voltage mode circuit implementation.

REFERENCES

[1] Smith K.C. and Sedra A. 1968. The current conveyor: a new circuit building block. IEEE Proc., Vol. 56, pp. 1368-1369.

[2] Sedra A. and Smith K.C. 1970. A second generation current conveyor and its application. IEEE Trans. Circuit Theory, pp. 132-134.

[3] Biolek D., Senani R., Biolková V. and Kolka Z. 2008. Active elements for analog signal processing: Classification, review, and new proposals. Radioengineering, Vol. 17, No. 4, pp. 15-32.

[4] Pathak J. K., Singh A. K. and Raj Senani. 2014. New multiplier/divider using a single Cdba. American Journal of Electrical and Electronic Engineering, Vol. 2, No. 3. pp.98-102.

[5] Wilson B. 1990. Recent developments in current conveyors and current mode circuits. IEE Proc. G, 132, pp.63-76.

[6] Fabre A. 1995. Third-generation current conveyor: a new helpful active element. Electronics Letters, Vol. 31, No. 5, pp.338-339.

[7] Acar C. and Ozoguz S. 1999. A new versatile building block: current differencing buffered amplifier suitable for analog signal processing filters. Microelectronics Journal, 30, pp.157–160.

[8] Acar C. and Sedef H. 2003. Realization of nth-order current transfer function using current differencing buffered amplifiers. Int. J. Electronics, Vol. 90, No. 4, pp.277-283.

[9] Ozoguz S., Toker A. and Acar C. 1999. Current-mode continuous-time fully-integrated universal filter using CDBAs. Electronics Letters, Vol. 35, No. 2, pp.97-98.

[10] Koksal M., Oner S. E. and Sagbas M. 2009. A new second-order multi-mode multi-funtion filter using a single CDBA. European Conference on Circuit Theory and Design, pp.699-702.

[11] Toker A., Özoˇguz S., Çiçekoˇglu O. and Acar C. 2000. Current-mode all pass filters using current differencing buffered amplifier and a new high- Q bandpass filter configuration. IEEE Trans. Circuit Theory & Sys.—II: Analog and Digital Signal Processing, Vol. 47, No. 9.

[12] Tarim N. and Kuntman H. 2001. A high performance current differencing buffered amplifier. 13th

International Conference on Microelectronics, pp.153-156.

[13] Palmisano G., Paluinbo G. and Pennisi S. 2000. High performance and simple CMOS unity-gain amplifier. IEEE Transactions on Circuits and Systems - I, Vol. 47, No. 3, pp.406-410.

[14] Tangsrirat W., Fujii N. and Surakampontorn W. 2002. Current-mode leapfrog ladder filters using CDBAs. IEEE International Symposium on Circuits and Systems, Vol. 5, pp.57-60.

[15] Tangsrirat W., Klahan K., Dumawipata T. and Surakampontorn W. 2006. Low-voltage NMOS-based current differencing buffered amplifier and its application to current-mode ladder filter design. International Journal of Electronics, Vol. 93, No. 11, pp.777-791.

[16] Abou-Allam, Manku T., Ting M. and Obrecht M. S. 2000. Impact of technology scaling on CMOS RF devices and circuits. Proceedings of the IEEE Custom Integrated Circuits Conference, pp.361–364.

[17] Steyaert M., Dehaene W., Craninckx J., Walsh M. and Real P. 1999. A CMOS rectifier-integrator for amplitude detection in hard disk servo loops. IEEE J. Solid-State Circuits, Vol. 30, No. 7, pp.743–751.

[18] Dumawipata T., Tangsrirat W. and Surakampontorn W. 2007. Low-voltage current differencing buffered amplifier using only NMOS transistors. International Symposium on Integrated Circuits, pp.123-126.

[19] Sawangaroml V., Tangsrirat W. and Surakampontom W. 2006. NPN-based current differencing buffered amplifier and its application. SICE-ICASE International Joint Conference.

[20] Cakir C. and Cicekoglu O. 2008. Low-voltage high-performance CMOS current differencing buffered amplifier (CDBA). Ph.D Research in Microelectronics and Electronics, Istanbul, pp. 37-40.

[21] Carvajal R. G., Torralba A., Ramírez-Angulo J., Tombs J. and Muñoz F. 2002. Compact low-power high slew-rate CMOS buffer for large capacitive loads. Electronics Letters, Vol. 38, No. 32, pp.1348-1349.

[22] Cakir C., Minaei S. and Cicekoglu O. 2009. Low-voltage low-power and high-swing current differencing buffered amplifier. Circuits and Systems and TAISA Conference, pp.1-4.

[23] Cakir C., Minaei S. and Cicekoglu O. 2010. Low voltage low power CMOS current differencing buffered amplifier. Analog Integr Circ Sig process, Springer, Vol. 62, No. 2, pp.237-244.

[24] Kanjanop A. and Kasemsuwan V. 2011. A low voltage class AB current differencing buffered amplifier (CDBA). International Symposium on Intelligent Signal Processing and Communication Systems, pp.1-5.

[25] Maheshwari S. and Khan I. A. 2004. Current-controlled current differencing buffered amplifier: Implementation and applications. Active and Passive Electronic Components, No. 4, pp.219-227.

[26] Bashir S. A. and Shah N. A. 2012. Voltage mode universal filter using current differencing buffered amplifier as an active device. Circuits and Systems, Vol. 3, pp.278-281.

[27] Alaybeyolu E., Guney A. and Kuntman H. 2013. A new CMOS ZC-CDBA realization and its new filter application. EuroCon, pp.1814-1820.