VOL. 10, NO. 16, SEPTEMBER 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

SIMULATION METHOD OF A PINNED PHOTODIODE WITH NO IMAGE LAG AND DARK CURRENT

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ABSTRACT

In this paper, the simulation method of a pinned photodiode (PD) with no image lag and dark current is proposed. The pinned PD has a shallow p+ layer on top of the conventional PD to create the pinning effect. The simulated PD has a one fifth of image lag compared with the conventional one, with much less dark current as well. Silvaco TCAD simulators, mostly ATLAS device simulator, have been used for simulation.

Keywords: CMOS image sensor, photodiode, pinned photodiode, image lag, dark current.

INTRODUCTION

Image sensor types can broadly be classified into a CCD (Charge-Coupled Device) and a CIS (CMOS Image Sensor). Since recently developed CISs are fabricated using standard CMOS process with no or minor modification, a CIS overcomes many shortcomings of the CCD, e.g., readout can now be very fast, and it consumes very low power and uses low operation voltage, while random access enables selective readout of regions-of-interest [1]. Also, due to using standard process, CISs spend lower cost and can be integrated with various CMOS circuits for image signal processing. Therefore, a CIS currently becomes the more dominant technology for image sensors.

A CIS can be classified largely into 3-transistor (3-T) active pixel sensor (APS) and 4-transistor (4-T) APS. While basic operation is similar, 4-T APS possess an additional transistor to transfer photo generated electrons from the photodiode (PD) to a floating diffusion (FD) node for readout. The PD fabricated with the standard CMOS process is generally an n+p- PD and it suffers from high image lag and dark current. To overcome the problem, p+np- PD called a pinned PD was introduced and is widely used in the 4-T APS for high image quality due to no image lag and dark current.

This paper will focus on the pn junction detectors and problems related with the implementation of them. Also, the simulation method of a pinned PD with no image lag and dark current is proposed. The rest of this paper is organized as follows. The pinned PD is introduced in Section II. The detailed implementation of the pinned PD is proposed in Section III. Section IV shows the experimental results. In Section V, we will conclude this paper.

PINNED PHOTODIODE

There had been a long debate about an undesirable image lag with n+p- PDs. The n-th field decay lag is expressed as follows [2].

$$v_{lag}^{(n)} = \frac{1}{\beta}\ln\frac{1-e^{-\beta(n+1)v_{bias}}-e^{-\beta(v_{in}+v_{bias})}+e^{-\beta(v_{in}+(n+1)v_{bias})}}{1-e^{-\beta n v_{bias}}-e^{-\beta(v_{in}+v_{bias})}+e^{-\beta(v_{in}+nv_{bias})}} \quad (1)$$

The explanation of this effect can be facilitated using the potential profiles. Figure-1 shows the cross-sectional view

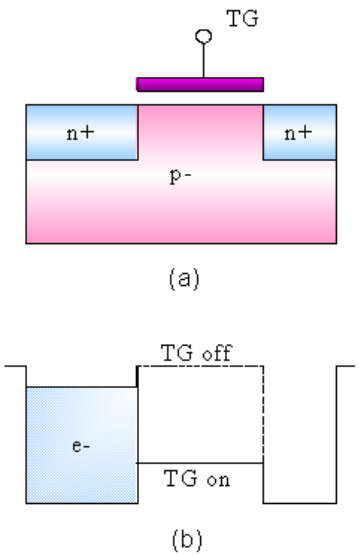

Figure-1. Conventional n+p- structure PD (a) cross-sectional view (b) potential profile.

and the potential profile of a conventional PD. At first, electron transfer from a PD to V-CCD mode through a transfer gate (TG) is done rapidly, due to the fact that the PD potential ψ_{PD} is low enough compared with the TG channel potential ψ_{TG}. When ψ_{PD} is sufficiently lowered so that it is larger than ($\psi_{TG} - \phi_{FP}$), the electron transfer is dominated by the sub threshold current. The transfer current we can be written as follows [3].

$$I = I_0(\psi_{TG})e^{-\beta\psi_{PD}} \qquad (\beta = \frac{q}{kT}) \tag{2}$$

As equation (2) indicates, the current cannot theoretically be completely transferred even with an infinite amount of time due to the exponential notation. With finite time intervals, like those used for PDs, the image lag problem becomes a greater issue.

To resolve this issue, PD structure can be modified to a p+np- structure. Doping concentration is carefully chosen so that the entire n layer is fully depleted [4]. The potential within the device is then fixed because no more

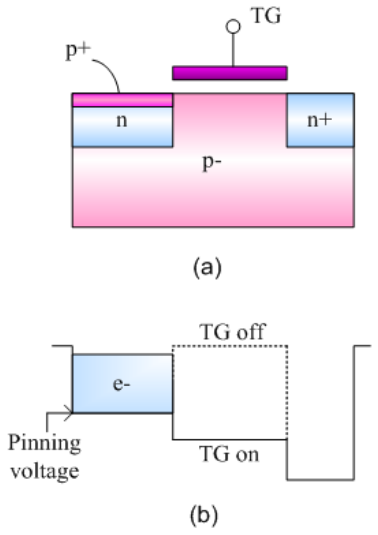

Figure-2. p+np- structure PD (a) cross-sectional view (b) potential profile.

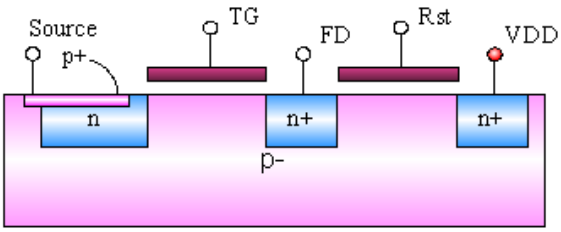

Figure-3. Simplified structure of the pinned PD.

majority carriers can be extracted from the device, leading to a finite ψ_{final} larger than ψ_{TG}. This accelerates the electron's transfer time from the PD to the readout circuit. p+ layer on top serves the purpose of enhancing the charge storage and capacity, eliminating carrier trapping, and eliminating dark current generation.

Often times, due to complexity of the process, fabrication of semiconductors does not appear to be aligned as they need to be. This causes unpredictable problems in the actual pixel. Having an unaligned PD and a TG is one of the main problems. When, due to misaligning, bare p- substrate between PD and TG is created, a small potential barrier between PD and TG is formed, as shown in Figure-2. This barrier hinders electron transfer, not as much as the conventional PD, but enough to leave an image lag. To make up for this problem, heavily doped n-region is introduced between PD and TG, compensating for a possible barrier. The doping is done in an angle and energy found experimentally.

IMPLEMENTATION

In the implementation of the pinned PD, Silvaco TCAD tools were used. Simulations are done on the device simulator ATLAS. Structures and other graphs were plotted using TONYPLOT software within the Silvaco TCAD bundle.

Structure Setting

First, the structure was created using ATLAS program. More nodes were added to allow the simulation.

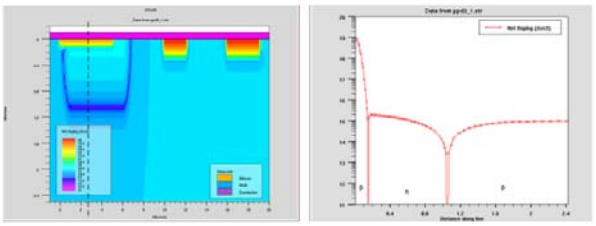

Figure-4. The pinned PD structure and the doping profile.

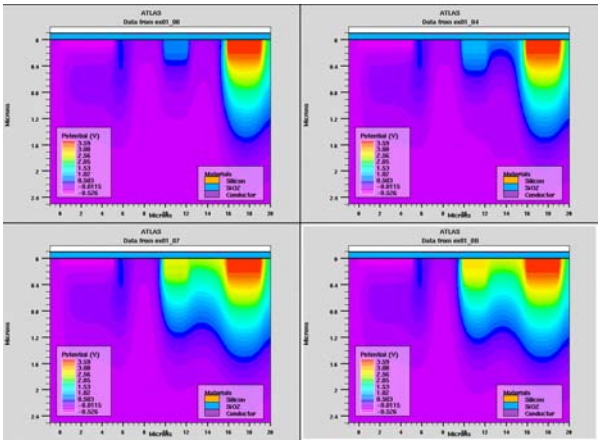

Figure-5. Turning on of the reset gate in a potential view.

FD node, the floating node where optically generated electrons would be transferred to and be read out, as well as the VDD and the reset gate are added. Figure-3 shows a simplified structure image of the PD to be simulated. The actual structure created using ATLAS is shown on Figure 4 with the cross-sectional doping profile. The cross-section was done along the dotted line on the

structure. The doping profile and the junction depth were carefully chosen to meet the pinning criterion. The size of the structure is 2.5 µm x 21 µm with initial p doping of 10^{15}. The p+ surface layer is from 0 to 5 and n layer from 1 to 6. The floating node was placed from 10 to 12 microns, and the VDD node was placed from 16 to 19. Both ends were given a micron of margin.

Charging of the Floating Diffusion Node

Once the structure has been set, the reset gate was opened to allow FD to charge up. FD would be charged to a potential of (VDD - V_{th}). The process is shown on Figure-5. The forming of channel, the potential shown in yellow below the reset gate, is apparent.

Once enough time has been allotted to fully charge the floating node, the reset gate is turned off. A phenomenon called feed through happens in the meanwhile. Feed through refers to a voltage drop caused by turning off of the gate. There exist parasitic capacitances between gate and source as well as gate and drain. As gate voltage changes, it would affect the capacitance in the FD node through parasitic capacitances between gate and other nodes. The voltage difference can be represented as follows.

$$\Delta v_1 = \frac{C_{gs}}{C_{FD} + C_{gs}}(v_{IN} + v_{th}) \quad (3)$$

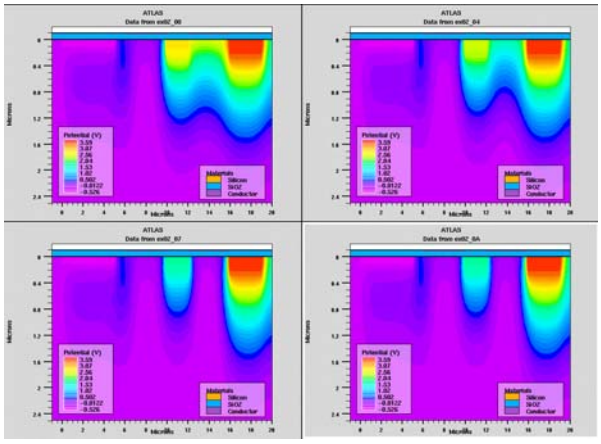

Figure-6. Turning off of the reset gate in a potential view.

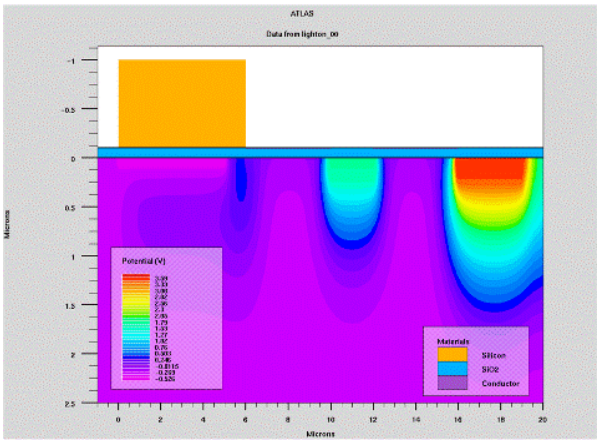

Figure-7. The position of the light irradiated.

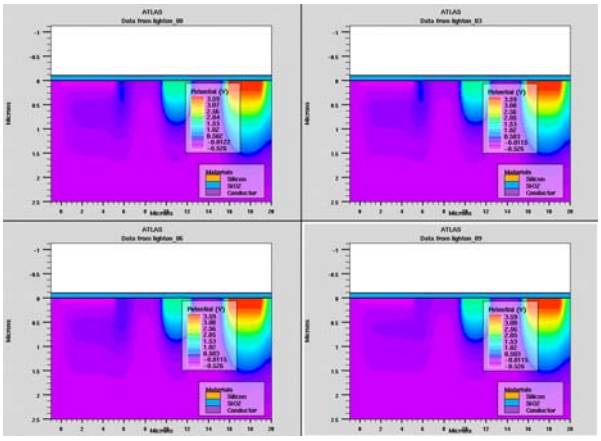

Figure-8. Irradiation for 4 ns.

In Figure-6, a potential diagram of turning off of the gate, feed through is observed by a slight change in the FD potential.

Irradiation

Light is irradiated only on the PD region of the structure - from 1 to 5 microns as shown in Figure-7. When new electrons were generated due to optical excitation, the potential of the area must go up a certain level. The voltage difference in the PD, although it may seem a bit small, is enough to bring about a voltage difference of 0.6 V in the floating node as shown in Figure-8. It is critical that the raised potential of the PD remains the same until the TG is opened, otherwise the potential difference would cause noise in the output image. In Figure-9, right diagram

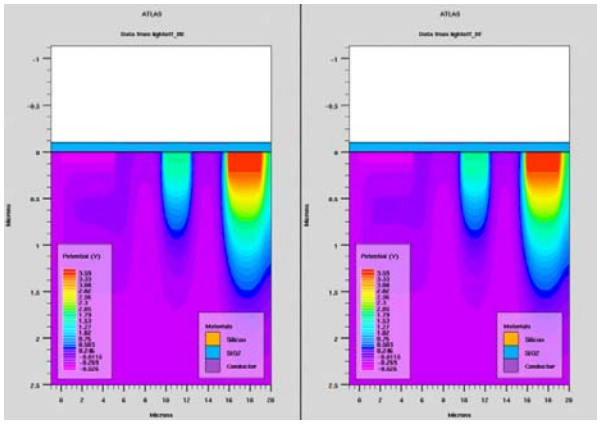

Figure-9. Potential in the PD after light has been turned off.

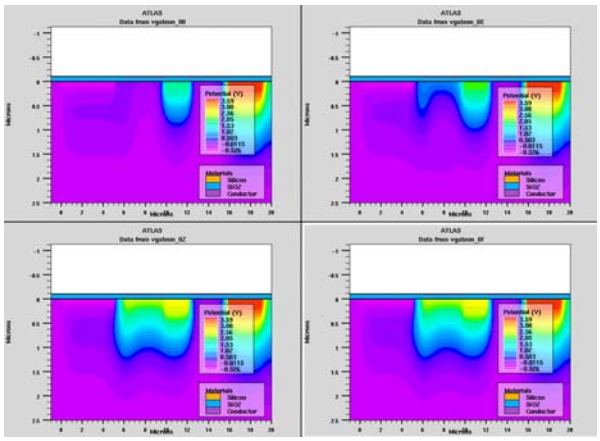

Figure-10. The potential diagram of the structure with TG on.

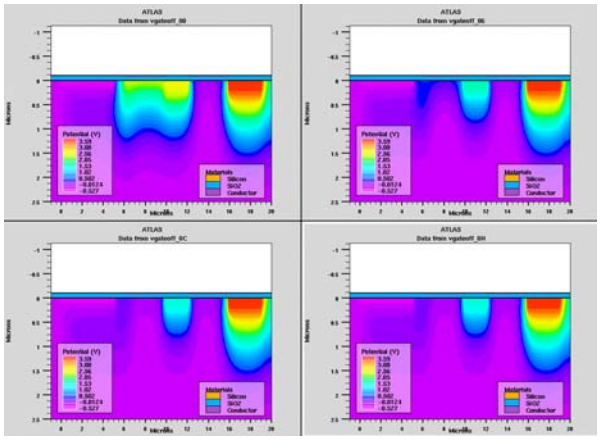

Figure-11. The potential diagram of the structure with TG off.

represents potential right after the light has been turned off and left diagram represents the potential right before the TG is turned on to allow charge transfer.

Charge Transfer

After the light irradiation, electron was generated by optical excitation. The excess electrons must then flow into the floating node to be readout. This is done by opening the TG. Just as when the reset gate is on, the channel

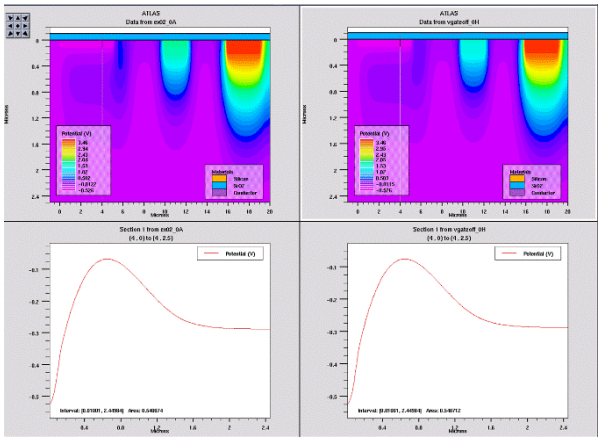

Figure-12. The potential change in the simulated pinned PD.

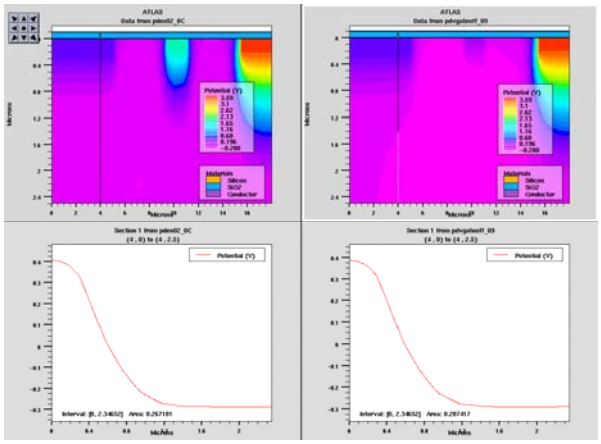

Figure-13. The potential change in the conventional PD.

formation under the TG is clearly visible as shown in Figure-10. Because of the feed through effect mentioned before, the floating node must be readout after the gate is turned off. In Figure-11, the potential diagram of the structure as the gate is turned off; the feed through can be observed again.

EXPERIMENTAL RESULTS

To correctly analyze the result, the same simulation process was done on the conventional PD. Two aspects of the pinned PD lag and dark current elimination has been checked.

Lag Elimination

To simulate the lag performance of the PD, the first idea that comes into mind is that it can be simulated by first going through the regular simulation, and then doing the same process again without light irradiation. This process, however, is quite time consuming. Considering the nature of pinned PDs and its operational principles, another method has been figured for lag elimination simulation. Because the simulated PD potential is pinned, PD returns to its original potential every time the excess electrons are transferred. With the conventional PD, once a light has been shed, there must remain a lag, producing a potential different from its original one. So to simulate the image lag, a pinned PD as well as a conventional one were simulated in the original process. The potential diagram of the finalized process has

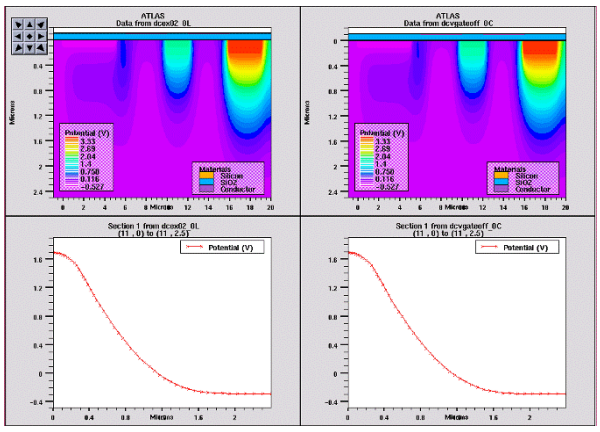

Figure-14. Potential of the floating node after dark current simulation in the pinned PD.

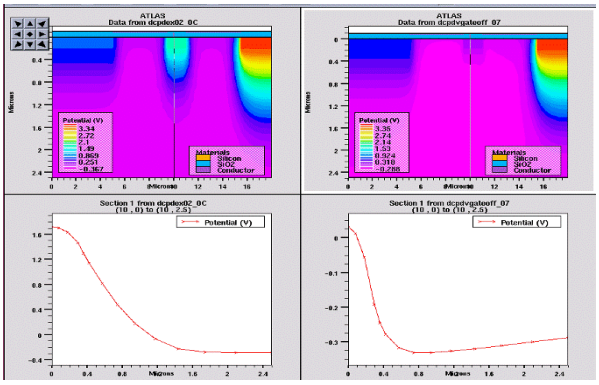

Figure-15. Potential of the floating node after dark current simulation in the conventional PD.

been compared with the potential diagram of the initial process, the one right after the charging of the floating node. The area of the potential cutline has been calculated to show the error - the lag.

Figure-12 shows the potential change before the irradiation and after the electron transfer. The error can be calculated as follows.

$$\left|\frac{V_{final} - V_{initial}}{V_{initial}}\right| \quad (4)$$

The error for pinned PD, therefore, is obtained as follows.

$$\left|\frac{0.548712 - 0.540074}{0.540074}\right| = 0.015994 \quad (5)$$

In case of the conventional PD, shown in Figure-13, the error is much greater. Calculated the same way, the error is obtained as follows.

$$\left|\frac{0.267181 - 0.287417}{0.267181}\right| = 0.075739 \quad (6)$$

It shows nearly a 20-fold decrease in the image lag.

Dark Current Elimination

To calculate the dark current of the PD, the same simulation process has been repeated without the light irradiation. To allow for thermal and other means of electron-hole pair generation, same time interval had been allowed. Figure-14 shows the dark current simulation of the pinned PD whereas Figure-15 shows the simulation of the conventional PD. Two images, when compared with each other, clearly show the elimination of dark currents in the pinned PD.

CONCLUSIONS

A pinned PD with no image lag and dark current has been simulated using Silvaco TCAD simulator. This PD has been created by having a shallow p+ layer on top of the conventional PD and decreasing the doping of underlying n layer. The n layer becomes fully depleted by the surface layer as well as the substrate p layer, creating a built-in potential throughout the layer. This potential layer leads to the formation of pinning phenomenon.

ACKNOWLEDGEMENT

This paper was supported by Research Fund, Kumoh National Institute of Technology.

REFERENCES

[1] H.-S. Wong. 1996. Technology and device scaling considerations for CMOS imagers. IEEE Trans. Electron Devices. 43(12): 2131-2141.

[2] N. Teranishi, A. Kohno, Y. Ishihara, E. Oda, and K. Arai. 1982. No image lag photodiode structure in the interline CCD image sensor. IEDM Tech. Dig. pp. 324-327.

[3] R. M. Swanson and J. D. Meindl. 1972. Ion-implanted complementary MOS transistors in low-voltage circuits. IEEE J. Solid-State Circuits. SC-7: 146-153.

[4] B. C. Burkey, W. C. Chang, J. Littlehale, T. H. Lee, T. J. Tredwell, J. P. Lavine, E. A. Trabka. 1984. The pinned phor/todiode for an interline-transfer CCD image sensor. IEDM Tech. Dig. pp. 28-31.