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# POWER ANALYSIS OF VOLATILE SRAM CELL IN DEEP SUB MICROMETER SCALE

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**ABSTRACT**

Leakage Power is a major problem in SRAM cell based FPGA's. The leakage power in FPGA is due to sub threshold leakage between source to drain and Gate to source oxide leakages. Due to drastic reduction of transistor size threshold voltage is also reduced exponentially, this in turn increases sub threshold leakages. Scaling trends of the transistor results in very thin gate oxide which in turn leads electrons tunneling through Gate oxide that result in Gate Oxide Leakage. By using Predictive technology Model parameters 16nm node SRAM cells are analyzed.

**Keywords:** sram cell, static noise margin, 16nm, predictive technology model.

## INTRODUCTION

Scaling of MOS transistor is the driving force of the semiconductor memory industry as the minimum feature size expected to go beyond 10nm in near future. SRAM cell plays vital role in high speed data storage devices. These SRAM cells are less stable in deep sub-micron scale, because of increasing leakage currents and non-ideal characteristics [1, 2]. As technological node shrinks, the demand for better functionality, low power consumption is also increases. However, power supply voltages remains around 1.0V even though process technologies continues in deep sub-micron technological nodes. Since power is a function of voltage, voltage scaling has become a major issue for CMOS technology [3]. voltage scaling is around 1.0 V at all the deep sub-micron nodes because of threshold voltage variation which is primarily caused by dopant fluctuation which is a form of device and process variation due to fluctuations in the concentration of the implanted dopant or impurity atoms in the MOS transistor channel [4]. Constant field scaling is keeps the electric field as constant and the supply voltage is reduced to a factor of K.

Predictive technology models (PTM) assess the behavior of the CMOS design through circuit simulation and it supports the early design prototyping. By using predictive Technology model power analysis is performed for 16nm SRAM cell. So the static and dynamic power measurement is required to analyze the transistor. Due to aggressive scaling of CMOS the limitation such as Drain induced barrier lowering (DIBL), sub threshold conduction, junction leakage is major problem [4]. To overcome these difficulties high - k dielectric, double gate devices need to use into conventional CMOS technology. Due to increasing leakage current in scaled devices, threshold voltage is not lowered much to avoid significant static power consumption [5]. Substantial leakage power reduction is achieved by reducing the threshold voltage and data retention voltage in SRAM cells. With 16nm PT model threshold voltage is reduced less than 1 volts.

## POWER DISSIPATION

In earlier, CMOS design power uses a secondary consideration behind area and speed. Due to advancement in scaling of transistors and increased clock frequency, power consumption has become primary design constraints.

In SRAM cell, power dissipation comes from two components:

(1) Static dissipation
(2) Dynamic dissipation. So,

$$P_{Total} = P_{Static} + P_{Dynamic} \quad (1)$$

As the static CMOS circuits are power efficient because the dissipation is nearly zero at idle state [4]. Due to increase in transistor count power consumption has also exponentially increases. Static power is a major concern in modern fabrication due to sub threshold conduction and tunneling current through gate oxides.

### Static Power Dissipation

Ideally, current flow in OFF transistor is zero, so the power dissipation is also zero. Zero quiescent dissipation is the main advantages of SRAN cell over other competing technologies. However secondary effects like sub-threshold conduction, leakage, tunneling, small amount of current flows through the OFF transistor.

The static power dissipation is the product of supply voltage & total leakage current.

$$P_{static=} Istatic \times V_{DD} \quad (2)$$

Static power is product of leakage current and supply voltage.

$$P_{static} = I_{static} * VDD \quad (3)$$

Sub threshold conduction current

$$I_{ds} = I_{ds0}\, e^{(Vgs - Vt/nVt)} (1 - e(-V_{ds}/V_t) \quad (4)$$

Where
$I_{ds0}$ = reverse bias drain to source current
$v_{ds}$ = drain to source voltage
n= Drain induced barrier lowering
$V_t$ = Threshold voltage

Tunneling current is important at deep submicron scale with gate oxide thickness of 20A or thinner.

$$V_t = V_{t0} - nV_{ds} + r\,(\Gamma\Phi_s + V_{sb} - \Gamma\Phi_s) \quad (5)$$

Where n = Drain induced barrier lowering
r = Body Effect

Sub threshold leakage power is major problem for battery operated devices. In a SRAM cell dynamic power dissipation is also important factor which affects performance. High Performance is expected when system is active and low leakage is expected when system is idle.

**Dynamic Power Dissipation**

Load capacitance is the primary source of dynamic power dissipation. The average dynamic power dissipation is

$$P_{dynamic} = c\, Vdd^2 f \quad \text{-------(6)}$$

$$P_{dynamic} = \alpha\, c\, Vdd^2\, f \quad \text{-------(7)}$$

Where α is activity factor

Activity factor is important, static logic has an inherently low activity factor. Voltage has a quadratic effect on dynamic power so by using 16nm predictive technology model low power supply is significantly reduces power dissipation. Dynamic power dissipation is usually reduced by decreasing the activity factor, switching capacitance and power supply voltages.

**T CMOS SRAM CELL**

An SRAM cell is consists of six MOSFETs. Each bit in an SRAM cell is stored on four transistors which forms two cross-coupled inverters. This cell has two stable states which are usually denoted as 0 and 1. Two additional access transistors are used to control the access to storage cell during read and write operations. Accessing the cell is enabled through the word line that controls the two access transistors $M_5$ and $M_6$ this, in turn, monitor whether the cell must be connected to the bit line and bit line bar. These two transistors are used to transfer data for both read and write operations. The necessity of placing two bit lines is to improve noise margins [6]. It uses bi stable latching circuitry to store each bit. It is volatile that data is lost when the memory is not powered.

The major operation of SRAM cell is hold, read, write, static noise margin is a performance factor of hold and read operations. During read operation the bit lines are driven high and low by the inverters in the SRAM cell [7, 9]. This operation improves SRAM bandwidth compared to its DRAM counterpart where the bit line is connected to storage capacitors and charging and discharging causes the bit line to swing up and down. Due to symmetric structure of SRAMs small voltage swings more easily detectable caused through differential signaling [8].

The size of a SRAM cell with *m* address and *n* data lines is $2^m$ words, or $2^m \times n$ bits. Single byte can be read or written to each of $2^m$ different words within the SRAM cell.

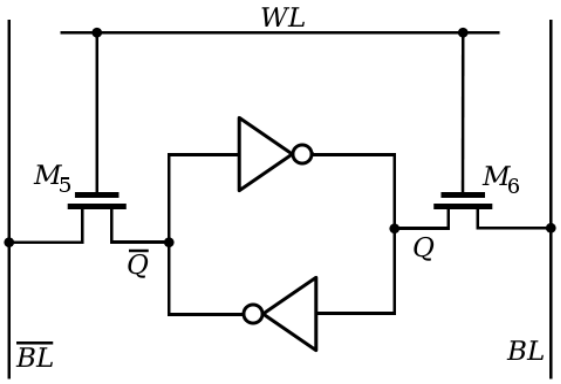


**Figure-1.** Cross coupled inverter SRAM.

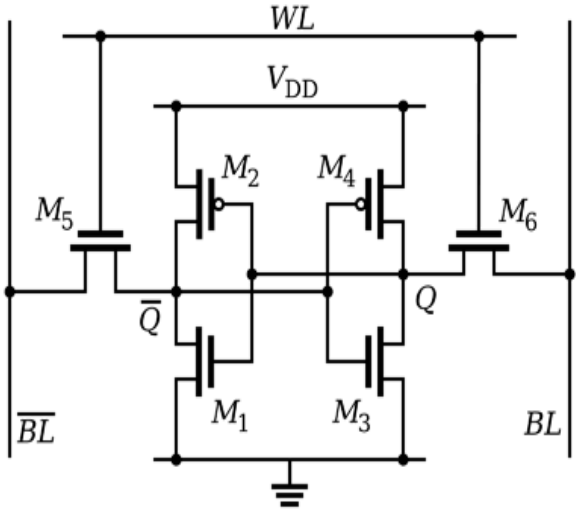


**Figure-2.** SRAM cell.

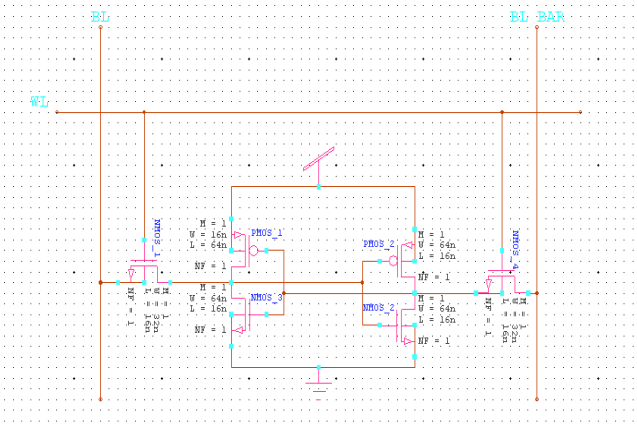


**Figure-3.** 6T SRAM cell using tanner.

**Read and Write**

Figure-2 shows CMOS inverter based operation of SRAM cell. Initially both bitlines are assumed to floated high voltages. Without loss of generality, assume Q is '0' and so Qbar is '1'. Qbar and bitbar both should remain '1'. When the word line is made high, bit should be pulled down through transistor M5 and M6. At that time bit is being pulled down, node Q tends to rise. Q is kept low by M3, but raised due to current flow from M6. So M3 must be stronger than M6. In order to do this, the transistors are ratioed such that node Q below the switching threshold of M4/M3 inverter.

In order to perform write operation let assume Q is initially '0' and '1' is to be written into the cell. BL is precharged to high and left floating, BLbar is pulled low. Due to read stability constraints the BL will not able to force Q high through M6 transistor. So the cell must be written by forcing Qbar through M5, M2 opposes this operation. So M2 must be weaker than M5, so Qbar can be pulled low. Now write ability is achieved. Once Qbar falls low, M3 is OFF, M4 is ON, this makes the Q as high. In order to ensure both read stability and write ability, the nmos pull-down transistor in the cross coupled inverters must be strongest. The accessing transistors are designed in intermediate strength and the pull up PMOS transistors must be week. In order to achieve good layout density, all the pull-down transistor are of 8λ/2λ, the access transistor are of 4λ/2λ and pull-up transistors are of 3λ/3λ.

**SRAM OPERATION**

An SRAM cell has three different state of operation. *Standby* (the circuit is idle), *reading* (the data request) and *writing* (updating the data). The three different states work as,

**Standby**

If the word line is low, the *access* transistors $M_5$ and $M_6$ disconnect the SRAM cell from the bit lines. The cross-coupled inverters will continue to reinforce each other as long as power is supplied.

**Reading**

To read the data the word line WL is asserted high and reading the SRAM cell state by a single access transistor and bit line [10]. The read cycle is charged by an external voltage such as both bit lines BL and BL, driving the bit lines to a threshold voltage .by asserting the word line WL, enabling both the access transistors M5 and M6 which causes that the bit line BL voltage either slightly drops or rises. the BL and BL bar lines will have a small voltage difference among them, which will sense which lines has the higher voltage thus determining whether there was one stored or 0.

**Writing**

Write cycle starts by applying the value to be written to the bit lines. One is written by inverting the values of the bit lines. WL is made high and the value that is to be stored is latched in. In practice, access transistors are to be stronger than either NMOS or PMOS transistors used in cross coupled inverters [11]. This is derived by same size of PMOS and NMOS transistors. When one transistor pair of transistors i.e., M3 and $M_4$ is slightly override by the write process, the opposite transistors pair i.e., $M_1$ and $M_2$ gate voltage is also changes. This leads M1 and $M_2$ transistors can be easily overrides. So the cross-coupled inverters perform the writing process.

**STATIC NOISE MARGIN OF SRAM**

Noise margin is related to the DC transfer curve of SRAM. The noise margin high and low is defined as

NM(high) =VoH - ViH ------(8)

NM(low) =VoL - ViL ------(9)

Where

ViL is the maximum input voltage level at logical '0',
ViH is minimum input voltage level at logical '0'
VoH is the minimum output voltage at logical '1',
VoL is the maximum output voltage at logical '1'

A major advantage of this method is that it can be generated using a DC circuit simulator. Here a SRAM cell is presented as two inverters are cross coupled.

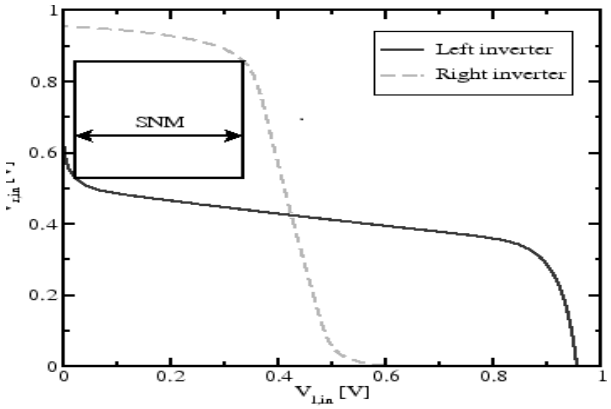


**Figure-4.** Static noise margin.

## SUMMARY OF RESULTS

In the Figure-6 read and write time delay is plotted by using predictive technology model by considering word and bit lines. Leakage power is low at 0.75 $I_{on}$ (mA/um) with $I_{off}$(A/um). The noise margin of the SRAM cell shows that DC power of the cells. In the Figure-6 the mask pattern of the SRAM cell is drawn and analyzed for power dissipation.

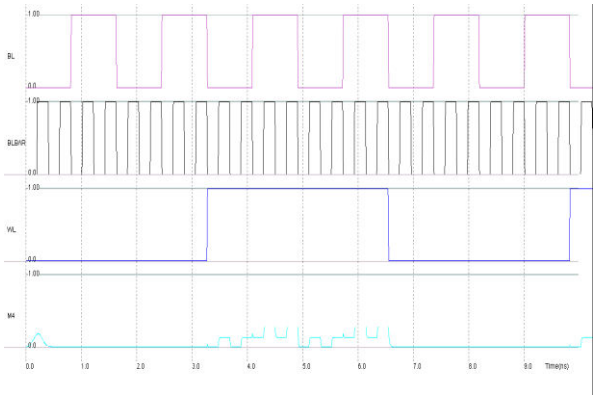

**Figure-5.** Read Write Cycle.

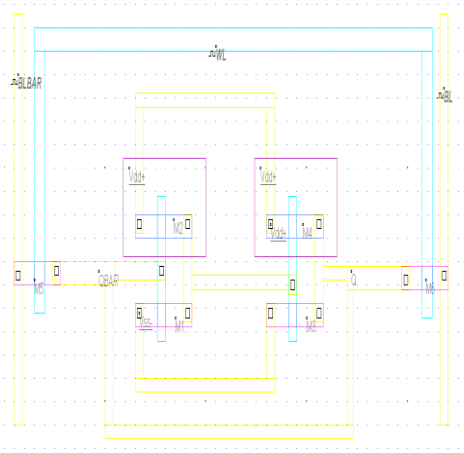

**Figure-6.** Mask structure of SRAM Cell.

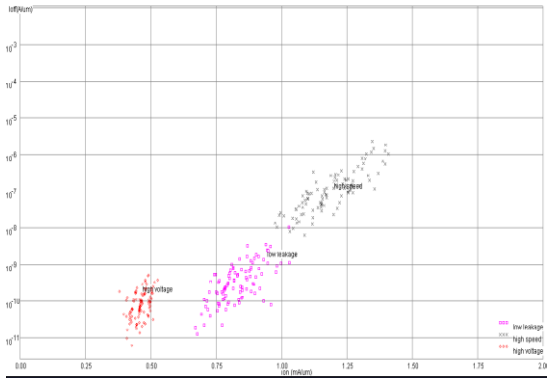

**Figure-7.** Low leakage power.

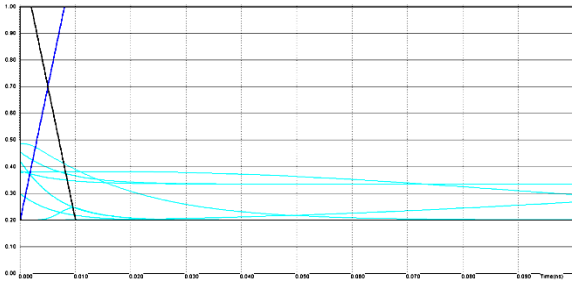

**Figure-8.** Noise margin.

**Table-1.** Read Write Delay.

| Parameters | Values |
|---|---|
| Average power consumed | 0.414 uwatts |
| Read delay | 2.845e-010 sec |
| Write delay | 7.521e-010 sec |
| Hold SNM | 0.7 volts |
| Read SNM | 0.2 volts |
| Write SNM | 0.9 volts |

## CONCLUSIONS

In this paper we have analyzed a 6T-based SRAM cell to address the critical issues in designing a low power static RAM in deep sub-micron technologies .we have preserved the existing SRAM architecture and the basic 6T SRAM cell structure was chosen to analyze. We have excluded the decoder, and MUX to implement. The access path of SRAM is split into two portions: from address line to word line rise and from word line rise to data output. By using Predictive technology model the leakage currents are addressed with an aid of using High K dielectric. The power consumption of each SRAM cell is measured Read and Write delay is analyzed with simulation results.

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