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VLSI ARCHITECTURE FOR SPECTRALLY EFFICIENT FREQUENCY DIVISION MULTIPLEXING TRANSMITTER

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ABSTRACT

Spectrally efficient FDM (SEFDM) systems can provide relative bandwidth savings and employ non-orthogonal overlapped carriers to improve spectral efficiency for communication systems in future. An approach is done for the implementation of SEFDM transmitter on FPGA .Non-orthogonal signals can be represented using Inverse Discrete Fourier Transform (IDFT) blocks that can be efficiently realized with the Inverse Fast Fourier transform (IFFT) algorithm. This is done for digital baseband transmitter architecture for SEFDM. For good throughput, multiple IFFTs are needed, which can be configured as parallel architecture is explained.

Keywords: OFDM, bandwidth compression factor, spectrally efficient FDM.

INTRODUCTION

Wireless communication has become essential for all aspects of our lives. Multi-carrier communications helps to facilitate increased utilization of wireless spectrum. There has been a great demand for bandwidth of multicarrier communication systems .Multi-carrier transmission or modulation (MCM) uses multiple carrier signals at different frequencies. The advantages of MCM include relative immunity to fading caused by transmission over more than one path at a time (multipath fading), less susceptibility to interference caused by impulse noise than single-carrier systems, and enhanced immunity to inter-symbol interference [1]. Orthogonal Frequency Division Multiplexing (OFDM) has been adopted mostly in present communication systems [2].Then the Spectrally Efficient Frequency Division Multiplexing (SEFDM) was proposed to overcome some disadvantages of OFDM [3]. But there are number of practical implementation challenges for SEFDM systems are there, such as the area minimization and power dissipation overheads.

There is importance of the Discrete Fourier Transform (DFT) in various digital signal processing applications. Fast Fourier transform (FFT) algorithms is an efficient algorithm for DFT that uses these two basic properties such as symmetry and periodicity [4]. DIF FFT algorithm is mainly used for spectrally efficient FDM.

OFDM is a multi-carrier modulation technique in which a single high rate data-stream is divided into multiple low rate data-streams and is modulated using subcarriers which are orthogonal to each other. This is the modulation technique that is increasingly being adopted in the telecommunication field. In this, the data to be transmitted is spread over a large number of orthogonal carriers, each being modulated at a low rate. OFDM has become the basis of many telecommunications fields which is widely used modulation and multiplexing technology [2, 5].

Sensitivity to frequency synchronization problems, high peak-to-average-power ratio (PAPR), requiring linear transmitter circuitry, loss of efficiency and poor power efficiency caused by cyclic prefix are the main problems .One of the most difficult engineering concerns in the RF portion of traditional OFDM modems is handling very large peak-to-average power ratios (PAPRs). This affects dynamic range of circuit. A peak in the signal power will occur when all, or most, of the sub-carriers are themselves aligned in phase. This will occur once every symbol period [1, 6]. These are the disadvantages of OFDM. The value of the PAPR is directly proportional to the number of carriers, and is given by [7, 8]:

$$\text{PAPR (dB)} = 10 \log (N) \quad (1)$$

Where, N is the number of carriers.

$$PAPR = max|x(t)|^2/E[|x(t)|^2] \quad (2)$$

However it has many challenges and disadvantages. [7, 8] pointed that there is possibility in OFDM that all subcarriers' power adding up constructively lead to a combined signal with a very high peak power and hence a high Peak to Average Power Ratio (PAPR) leading to a distorted signal. They are very sensitive to frequency errors and there will be inter-carrier interference (ICI) between the subcarriers. The techniques to reduce PAPR can be used to reduce the PAPR at the cost of loss in data rate, transmit signal power increase, BER performance degradation, computational complexity increase, and so on [7].

To overcome these disadvantages of OFDM a new concept known as SEFDM was introduced [3].The Spectrally Efficient Frequency Division Multiplexing (SEFDM) system was proposed as a multicarrier modulation scheme that helps in better bandwidth utilization than an equivalent OFDM system . SEFDM achieves spectral savings by reducing the spacing of the subcarriers [3, 9]. But the orthogonality rule is violated. So, the complexity of the circuit would increase. According to [10], for digital generation of the SEFDM signal, it is said that that IDFT algorithm could be

performed economically with the Fast Fourier Transform (FFT) algorithm. Also, this will help in reduced cost of the system and reduced power consumption.

SEFDM system promises better utilization of bandwidth than Orthogonal Frequency Division Multiplexing (OFDM) system. SEFDM achieves spectral savings by reducing the spacing of the subcarriers [9].The aim is on developing high performance systems at low complexity.

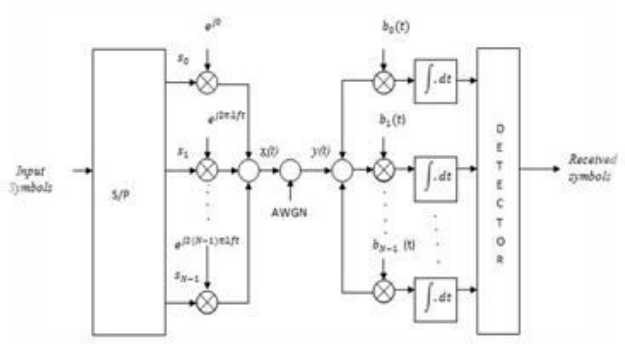


Figure-1. Block diagram of SEFDM.

The SEFDM signal consists of a stream of SEFDM symbols each carrying a block of N complex input symbols, denoted by
$s = s_R + js_I$, transmitted within T seconds. The time domain representation of a single frame of an SEFDM signal denoted by x(t) is given by

$$x(t) = (1/\sqrt{T})\left(\sum_{n=0}^{N-1} s_n e^{\frac{j2\pi nat}{T}}\right) \times g(t) \quad (3)$$

A discrete representation of SEFDM signals can be obtained by sampling each SEFDM frame, shown in (3) above, at a rate. Thus, a single discrete SEFDM will be given by

$$X(k) = 1/\sqrt{N}\left(\sum_{n=0}^{N-1} s_n e^{j2\pi nk\alpha/N}\right) \quad (4)$$

where k=1,2,3,…..N. SEFDM signal can be generated based on IDFT operations as explained in [4]. Here, α denotes the bandwidth compression factor defined as

$$\alpha = \Delta f \; T \quad (5)$$

Here, $\alpha < 1$. The frequency distance between the subcarriers is denoted by Δf, T is the SEFDM symbol duration, N is number of subcarriers and s denotes the symbol modulated on the nth subcarrier in the lth SEFDM symbol [3,11, 12].

The fraction α determines the level of the bandwidth compression, thus termed bandwidth compression factor with α= 1 corresponding to an OFDM signal. Figure-3 depicts the spectra of an N subcarrier SEFDM system. Due to the relatively closer locations of the subcarriers in frequency, the spectral width of the multiplexed signal is narrower than that of OFDM. In [1, 12, 13] the bandwidth and spectra of OFDM and SEFDM have been compared. The bandwidth occupied by the SEFDM system is approximately equal to

$$BW_{SEFDM} = (\alpha(N-1)+2)/2 \quad (6)$$

Whereas N subcarrier OFDM system has a bandwidth equal to

$$BW_{OFDM} = (N+1)/2 \quad (7)$$

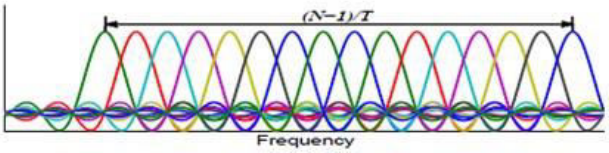


Figure-2. OFDM Spectra with N carriers.

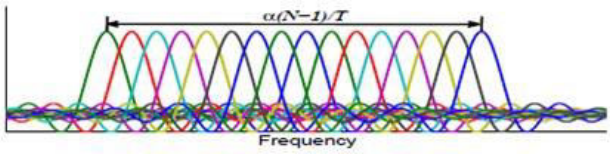


Figure-3. SEFDM Spectra with N carriers.

This shows that the occupied bandwidth of the SEFDM system approaches α of the OFDM bandwidth with the increase in N as explained in [14] multiple shorter IDFTs are used in place of one large IDFT. The overall complexity of the system is expected to decrease as it uses multiple parallel shorter IDFT compared to the design that uses single block of IDFT. The scheme could be especially useful for systems with large numbers of carriers as it becomes less feasible to use very long IDFT to generate the signal. By expressing the term α as a rational number[11], that is by taking α=b/c and b<c, here b and c are integers, the SEFDM expressed as :

$$X[k] = 1/\sqrt{N}\left(\sum_{n=0}^{cN-1} s_n' e^{j2\pi nkb/cN}\right) \quad (8)$$

As for the case above, here we define S' to be a vector of length c N whose elements s_i take the values of either the input symbols or zeros as

$$S' = \begin{cases} S_{i/b}, i \in I \\ 0, \quad otherwise \end{cases} \quad (9)$$

Let I={0,b, ……b(N-1)}above equation can be expressed by n = i + mc,

$$X[k] = 1/\sqrt{N}\left(\sum_{n=0}^{c-1} e^{j2\pi ib/(cN)} + \sum_{i=0}^{N-1} s'_{i+mc} e^{j2\pi mk/N}\right) \quad (10)$$

shows that the samples of the SEFDM signal can be generated using c IDFT operations each of length of N points. SEFDM can be used in cable and wireless communications, digital subscriber line broadband access

as well as digital video broadcasting and for high speed local area networking.

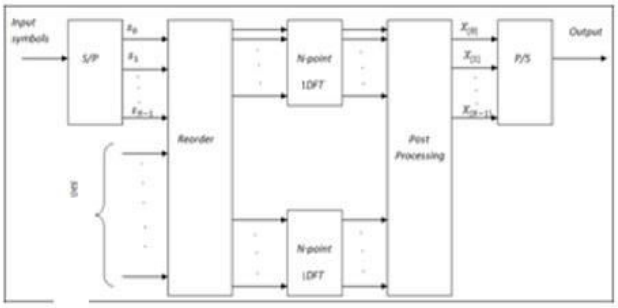


Figure-4. SEFDM IDFT based transmitter.

SEFDM TRANSMITTER AS VLSI ARCHITECTURE

The modulator does operations such as zero-insertion and reorder. The IFFTs and post-processing are the other blocks [11], as discussed individually in the following sections.

Zero Insertion

This stage consists of padding the input symbols with zeros before inputting to the IFFT block .The output can be data or zeroes depending on the control signal.

IFFT Block

The 64-point, IFFT block based on the radix flow graph is used. Multiple shorter IDFTs are used in place of one large IDFT in Figure-4. The overall complexity of the system is expected to decrease as it uses multiple parallel shorter IDFT compared to the design using single IDFT block [10,14] .One of the famous FFT architecture is single path delay feedback. This is used in IFFT block of SEFDM. Pipeline FFT processor [15] is a specified class of processors for DFT computation utilizing fast algorithms. It is of real-time and non-stop processing as the data sequence passes through the processor. [16] points out that single-path delay feedback uses the registers more efficiently by storing the one butterfly output in feedback shift registers. At every stage a single data stream goes through the multiplier. It has same number of butterfly units and multipliers as in multipath delay commutator approach, but with much reduced memory requirement: *N* - 1 registers. Its memory requirement is minimal. On first N/2 cycles, the 2-to-1 multiplexers in the first butterfly module switch to position '0', and the butterfly is idle. The input data from left is directed to the shift registers until they are filled. On next N/2 cycles, the multiplexers switch to position '1', the butterfly computes a 2-point DFT with incoming data and the data stored in the shift registers[17].

$$Z1(n) = x(n) + x(n+(N/2)) \quad (11)$$

$$Z1(n + N/2) = x(n) - x(n+(N/2)),\ 0<n < (N/2) \quad (12)$$

Post-Processing

The post-processing block. Here, modified booth algorithm using modified booth encoder [18] is used to multiply the output of the IFFT block with the input gain. The sparse Kogge-Stone adder [19, 20] is used to add partial products. This adder generates lesser no of carriers compared to regular Kogge-Stone adder.

PARALLEL SEFDM TRANSMITTER ARCHITECTURE

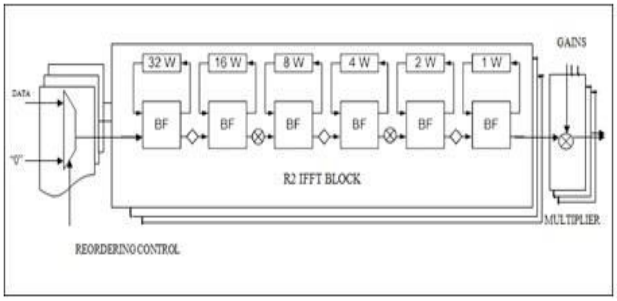


Figure-5. Parallel SEFDM transmitter architecture, consisting of input reorder logic, parallel IFFTs and post processing complex multipliers.

Figure-5 shows the block diagram of Parallel SEFDM transmitter architecture, consisting of input reorder logic, 3 parallel IFFTs and post processing multipliers.BF indicates butterfly operation. Using parallel IFFTs allows the highest throughput at the cost of linear increase in area [3].

MULTI-STREAM IMPLEMENTATION OF SEFDM TRANSMITTER

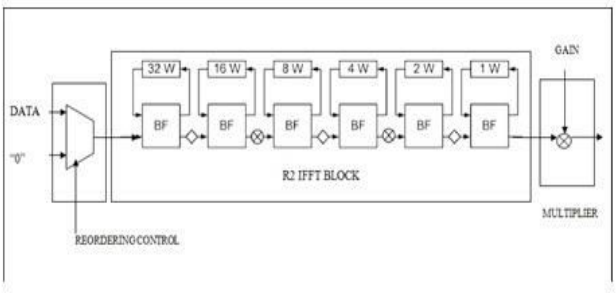


Figure-6. Multi-stream implementation of SEFDM transmitter consisting of input reorder logic, multi-stream IFFTs[1] and post processing multipliers.BF indicates butterfly operation.

Figure-6. shows the block diagram of multi-stream implementation of SEFDM transmitter consisting of input reorder logic, multi-stream IFFTs and post processing multipliers.BF indicates butterfly operation. This architecture is more suited to area constrained designs. The multi-stream IFFT accepts samples from input stream, such that transformed output samples appear at the output [3].

RESULTS

The simulation of both architectures discussed is done using Xilinx ISE Simulator) using Verilog language. Spartan 6 FPGA is used as hardware.

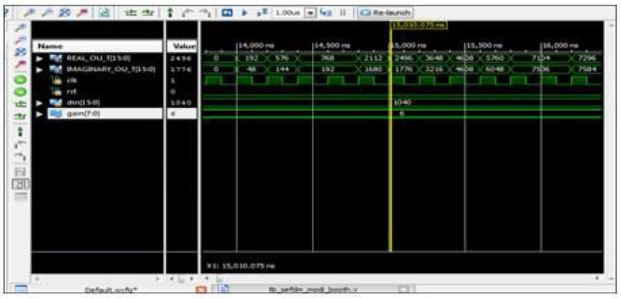
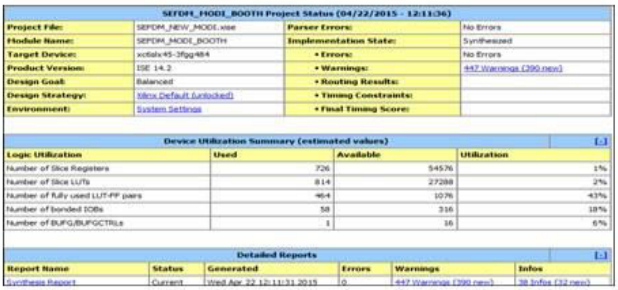


Figure-7. Simulation of multi-stream SEFDM architecture.



SEFDM_MODI_BOOTH Project Status (04/22/2015 - 12:11:36)			
Project File:	SEFDM_NEW_MODE.xise	Parser Errors:	No Errors
Module Name:	SEFDM_MODE_BOOTH	Implementation State:	Synthesized
Target Device:	xc6slx45-3fgg484	• Errors:	No Errors
Product Version:	ISE 14.2	• Warnings:	447 Warnings (390 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	726	54576	1%
Number of Slice LUTs	814	27288	2%
Number of fully used LUT-FF pairs	464	1076	43%
Number of bonded IOBs	58	316	18%
Number of BUFG/BUFGCTRLs	1	16	6%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed Apr 22 12:11:31 2015	0	447 Warnings (390 new)	38 Infos (32 new)

Figure-8. Device utilization summary of multi-stream SEFDM architecture.

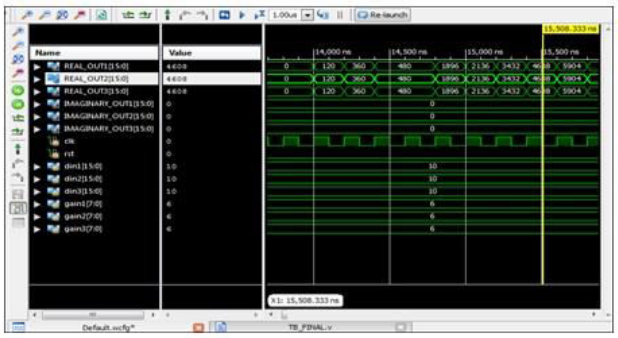


Figure-9. Simulation of parallel SEFDM architecture.

SEFDM_MODI_BOOTH Project Status (04/22/2015 - 12:07:47)			
Project File:	SEFDM_NEW_MODE.xise	Parser Errors:	No Errors
Module Name:	FINAL_SEFDM_MULT	Implementation State:	Synthesized
Target Device:	xc6slx45-3fgg484	• Errors:	No Errors
Product Version:	ISE 14.2	• Warnings:	1279 Warnings (1170 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	2070	54576	3%
Number of Slice LUTs	2294	27288	8%
Number of fully used LUT-FF pairs	1283	3081	41%
Number of bonded IOBs	170	316	53%
Number of BUFG/BUFGCTRLs	1	16	6%

Figure-10. Device utilization summary of parallel SEFDM architecture.

CONCLUSIONS

Spectrally efficient FDM (SEFDM) systems can provide relative bandwidth savings and employ non-orthogonal overlapped carriers to improve spectral efficiency for communication systems in future. An approach is done for the implementation of SEFDM transmitter on FPGA Inverse Discrete Fourier Transform (IDFT) blocks can be used to represent non-orthogonal signals that can be efficiently realized with the Inverse Fast Fourier transform (IFFT) algorithm for digital baseband transmitter architecture for SEFDM. Parallel transform architecture using multiple FFTs used for good throughput and multistream architecture can be used for reduced circuit area.

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